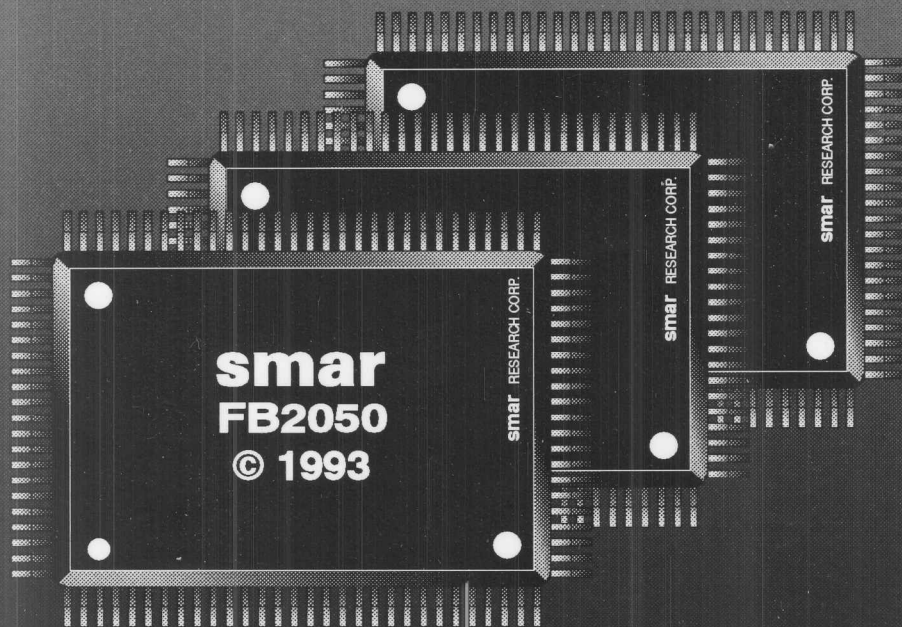




FIELDBUS COMMUNICATION PRODUCTS

smar SEMICONDUCTORS

FIELD BUS COMMUNICATION PRODUCTS

smar SEMICONDUCTOR

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PRELIMINARY INFORMATION

April/94

CHAPTER I-A

Datasheets FB1050

PRELIMINARY INFORMATION

SMAR FB1050 FIELDBUS COMMUNICATION CONTROLLER

- Manchester Encoder/Decoder Built in
- Supports Fieldbus Mode Full Duplex Communication
- Based on Fieldbus Standard for use in Industrial Control ISA-SP50.02-1992-Part 2, Physical Layer Definition.
- Low Power Consumption, Typically Less than 1.5 mA
- Data Rates at 31.25 Kbits/s
- Available in 44-pin PLCC
- Synchronous 8-bit Characters; Internal Character Synchronization; Automatic Synch Insertion/ Detection (start of header, end of header)
- Error Detection on Missing Manchester Symbols
- Temperature Range: -40° C to +85° C
- Automatic Polarity Detection and Correction
- Compatible with Most Microprocessors and Micro-controllers

The SMAR FB1050 is a synchronous receiver/transmitter communication controller. It is designed to implement the physical layer of the Fieldbus Communication Standard for use in industrial control systems. The SMAR FB1050 is used as a peripheral device with a CPU. It can receive data from the CPU in parallel and transmit them serially. At the same time, it can receive data serially from other devices and present them to the CPU in parallel. The status of the chip can be checked by the CPU, at any time, via the OVR, DVAL, TDRE, and RDRF pin flags. Figure 1 is the Block Diagram for this controller.

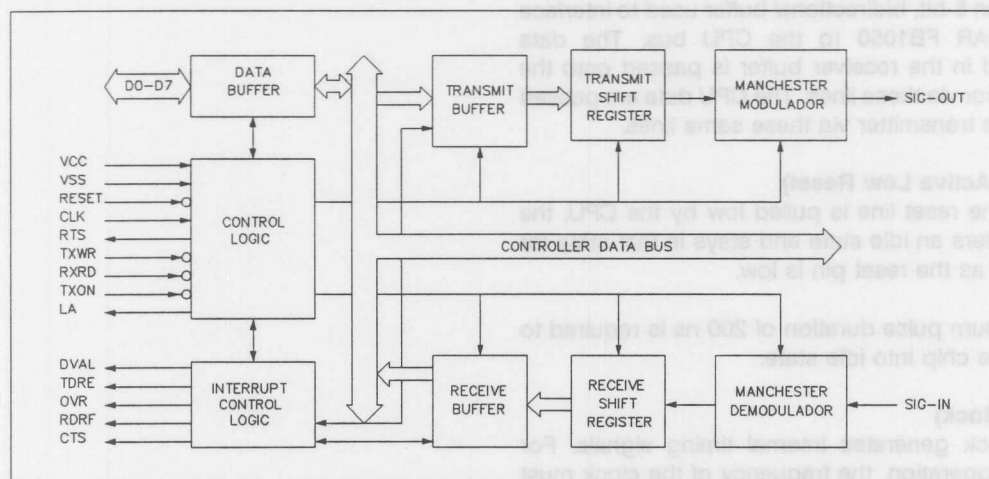


Figure 1 - Block Diagram

FUNCTIONAL DESCRIPTION

GENERAL

The SMAR FB1050 is a synchronous transmitter/receiver communication controller designed to be interfaced with most common microprocessors and microcontrollers. It is based on the ISA-S50.02-1992-Part 2 Fieldbus physical layer definition. In this communication environment, parallel data is converted to serial and is transmitted using Manchester encoding. Received data is converted from Manchester code into 8-bit parallel bytes and presented to the CPU. With the SMAR FB1050, the conversion process, as well as all other operations of the chip, is totally transparent to the CPU. The CPU regards the FB1050 as an I/O port. Table 1 contains the signal names, type, pin number and pin description of the FB1050 chip. Following is a more detailed description of the pin signals.

GENERAL SIGNALS:

D0 through D7 (Data Bus Buffer)

This is an 8-bit, bidirectional buffer used to interface the SMAR FB1050 to the CPU bus. The data received in the receiver buffer is passed onto the processor via these lines. The CPU data are passed onto the transmitter via these same lines.

Reset (Active Low Reset)

When the reset line is pulled low by the CPU, the chip enters an idle state and stays in that state for as long as the reset pin is low.

A minimum pulse duration of 200 ns is required to force the chip into idle state.

CLK (Clock)

The clock generates internal timing signals. For proper operation, the frequency of the clock must be at 20 times the data rate desired. For low speed Fieldbus application, CLK = 625 KHz.

RXRD (Receiver Read Data)

With low on this input signal, the FB1050 will write the contents in the receiver buffer into the data bus.

TXWR (Transmitter Write)

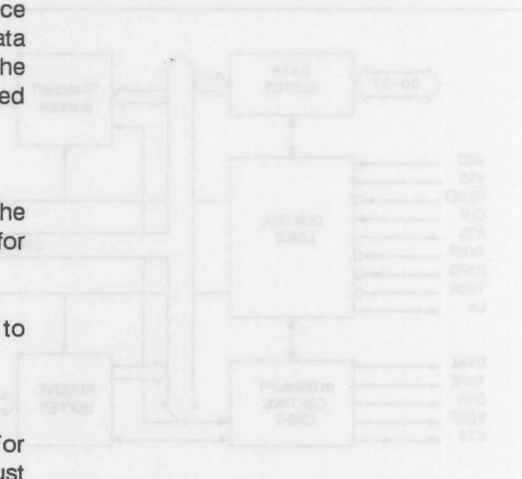
With low on this input signal, the FB1050 will write the contents in the data bus into the transmitter buffer.

SIG-OUT (Transmitter Fieldbus Signal Out)

This is the transmitter's modem digital output signal. During the idle state, this output is high. This output should be connected to Media Attachment Unit (MAU) which is a wave shaping filter and a current (or voltage) modulator attached to the transmission media or the Fieldbus lines.

SIG-IN (Receiver Fieldbus Signal In)

This is the digital input connected to the receiver demodulator. This pin should be connected to the Media Attachment Unit which is an input filter connected to an analog comparator.



PINOUT SUMMARY

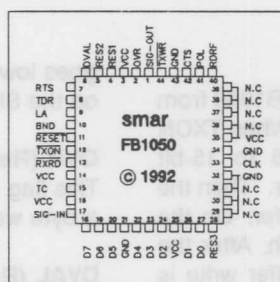


Figure 2 - FB1050 Pin Diagram (see Table 1)

SIGNAL NAME	TYPE	PIN N°.	PIN DESCRIPTION
SIG-OUT	O	1	TRANSMITTER; FIELDBUS SIGNAL OUT
OVR	O	2	RECEIVER; OVERRUN
RES1	O	4	RECEIVER; CLOCK RESET SYNC
RES2	O	5	RECEIVER; START OF HEADER
DVAL	O	6	RECEIVER; DATA VALID
RTS	O	7	TRANSMITTER; REQUEST TO SEND
TDRE	O	8	TRANSMITTER; DATA REGISTER EMPTY
LA	O	9	RECEIVER; LINE ACTIVITY
/RESET	I	11	RESET (L)
TXON	I	12	TRANSMITTER; ON (L)
RXRD	I	13	RECEIVER; READ DATA (L)
TC	O	15	TRANSMITTER; CLOCK @31.25KHz
SIG IN	I	17	RECEIVER; FIELDBUS SIGNAL IN
D7	I/O	18	DATA BIT 7
D6	I/O	19	DATA BIT 6
D5	I/O	20	DATA BIT 5
D4	I/O	22	DATA BIT 4
D3	I/O	23	DATA BIT 3
D2	I/O	24	DATA BIT 2
D1	I/O	26	DATA BIT 1
D0	I/O	27	DATA BIT 0
RES3	O	28	RECEIVER; END OF HEADER
CLK	I	33	CLOCK IN; 526 KHz
RDRF	O	40	RECEIVER; DATA REGISTER FULL
POL	O	41	RECEIVER; DATA POLARITY, H=POS
CTS	O	42	CLEAR TO SEND
/TXWR	I	44	TRANSMITTER; WRITE (L)
Vcc	+5 VDC	3 14 16 25 35	
GND	GROUND	10 21 32 34 43	
N.C.	---	29 30 31 36 37 38 39	

Table 1 - Pin Descriptions

Modulator Control Pins:

TXON (Transmitter On)

This active low input signal drives the FB1050 from idle state into the transmission state. When TXON goes high, the SIG-OUT sends an 8 to 15-bit preamble, followed by the start delimiter. Then the data is written into the transmitter buffer. On the negative edge of TXON, RTS goes high. After the rising edge of TXON, a transmitter buffer write is recommended; this should be done before the end of the preamble transmission.

RTS (Transmitter Request To Send)

This output signal goes high on the falling edge of TXON and remains high until the last bit of the data message is sent. It goes low when the transmission is complete.

CTS (Clear To Send)

When the first bit of the data is transmitted, this output data goes high. Note that preambles and delimiters are not considered to be part of the data. CTS goes low as soon as the last bit of data is transmitted.

TDRE (Transmitter Data Register Empty Flag)

This flag goes high when the transmitter data register is empty. The transmitter data register is empty when data is transferred from the transmitter buffer into the transmitter shift register. This is done automatically. TDRE goes low when this transfer takes place. TDRE can be used as a transmitter interrupt request or as a general purpose polling line. If the CPU fails to write to 14 transmitter data register within 8 bits of time space, the modulator will underrun and start the end-of-message procedure.

Demodulator Control Pins:

LA (Receiver Line Activity)

This output pin signals Fieldbus activity on the line. It goes high when a high-to-low transition followed by a low-to-high transition is detected on the line. It

goes low after six missing transitions are detected on the SIG-IN line.

OVR (Receiver Overrun Flag)

This flag goes high when the demodulator detects a byte was lost by the CPU.

DVAL (Receiver Data Valid Flag)

This flag goes high after successful reception of Start Delimiter. It goes low after the first missing Manchester symbol (N+ or N-). For successful communication this missing Manchester symbol should be part of the end delimiter character.

RDRF (Receiver Data Register Full Flag)

This flag goes high to indicate the transfer of a valid byte between the receiver shift register and the receiver buffer. It goes low when the RXRD signal goes low. RDRF can be used as an interrupt request line to signal the CPU to start reading the received byte.

TIMING DIAGRAMS

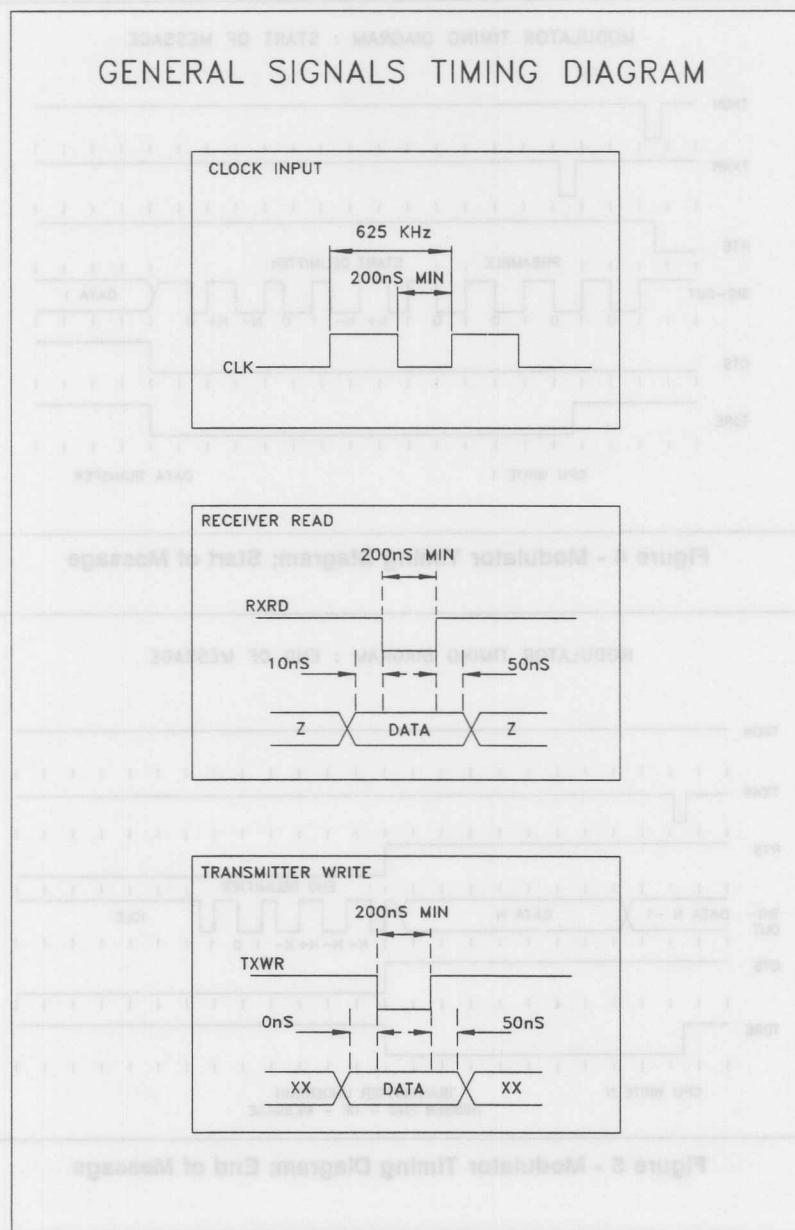


Figure 3 - General Signals Timing Diagram

TIMING DIAGRAMS

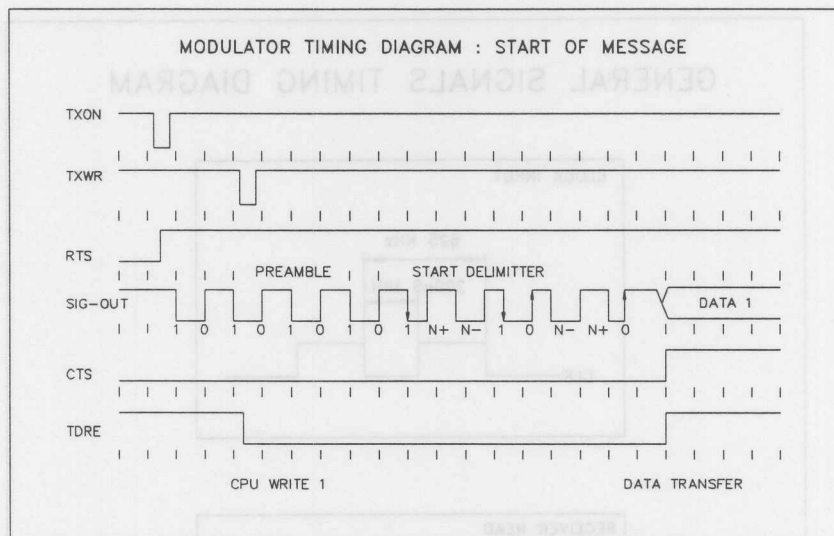


Figure 4 - Modulator Timing Diagram; Start of Message

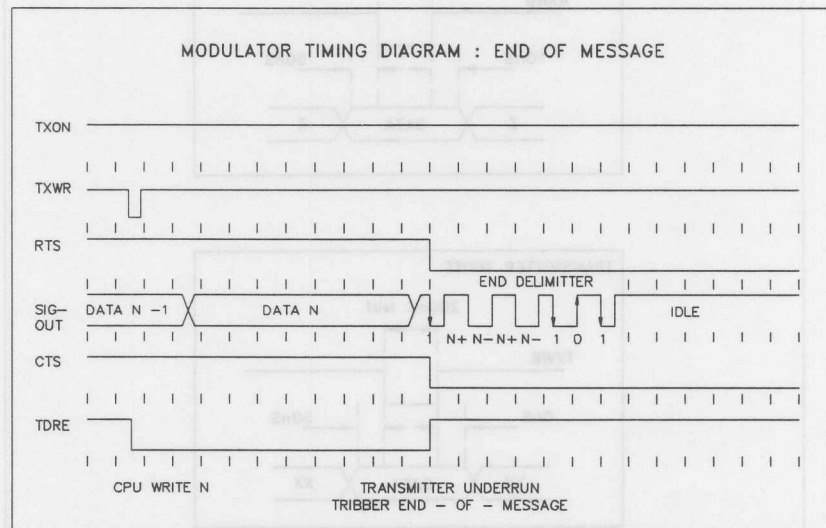


Figure 5 - Modulator Timing Diagram; End of Message

TIMING DIAGRAMS

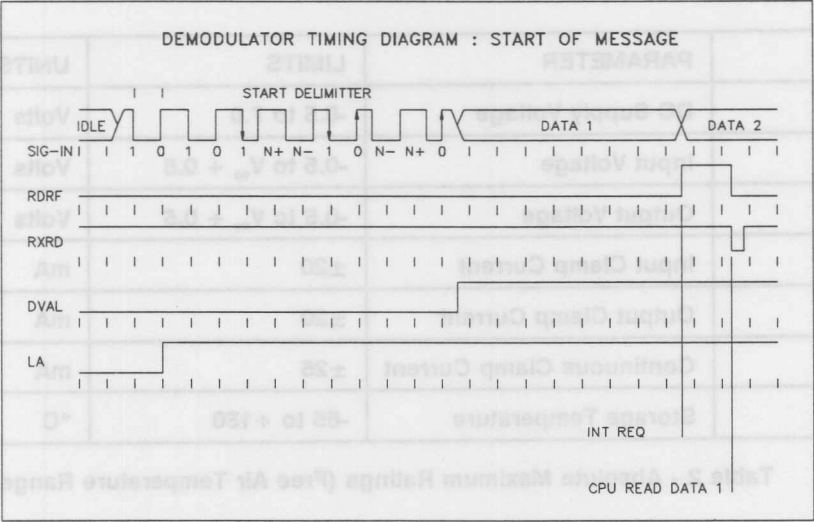


Figure 6 - Demodulator Timing Diagram; Start of Message

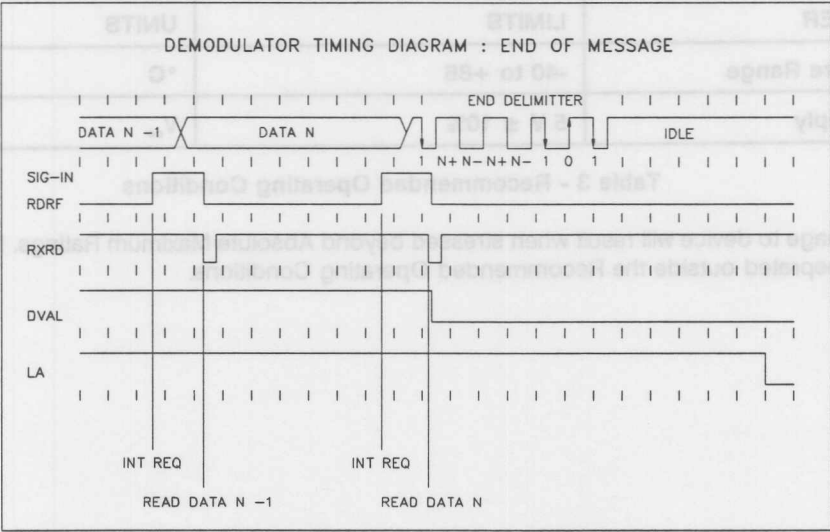


Figure 7 - Demodulator Timing Diagram; End of Message

ELECTRICAL SPECIFICATIONS

SYMBOL	PARAMETER	LIMITS	UNITS
V_{cc}	DC Supply Voltage	-0.5 to 7.0	Volts
V_i	Input Voltage	-0.5 to $V_{cc} + 0.5$	Volts
V_o	Output Voltage	-0.5 to $V_{cc} + 0.5$	Volts
I_{IK}	Input Clamp Current	± 20	mA
I_{OK}	Output Clamp Current	± 20	mA
I_{OK}	Continuous Clamp Current	± 25	mA
T_{STG}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$

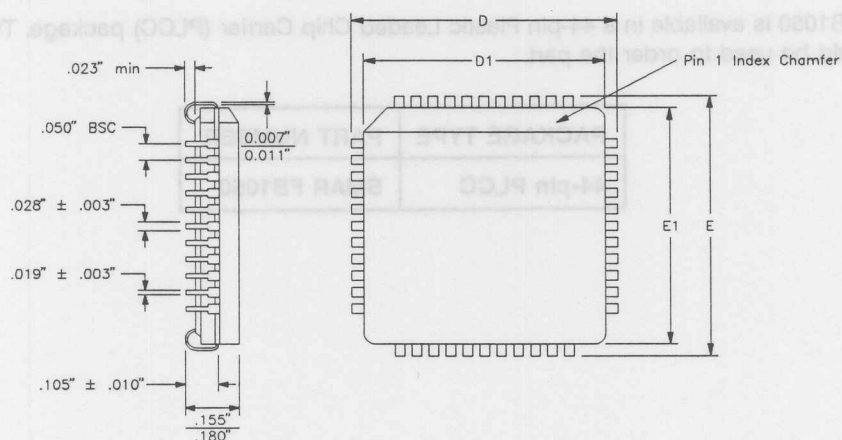
Table 2 - Absolute Maximum Ratings (Free Air Temperature Range)

PARAMETER	LIMITS	UNITS
Temperature Range	-40 to +85	$^{\circ}\text{C}$
Power Supply	5 V $\pm$ 10%	V_{cc}

Table 3 - Recommended Operating Conditions

NOTE: Damage to device will result when stressed beyond Absolute Maximum Ratings. Device should not be operated outside the Recommended Operating Conditions.

MECHANICAL SPECIFICATIONS



Lead Count	D, E	D1, E1
44	.690" ± .005"	.650" ± .008"

Figure 8 - 44-Pin J-Leaded Chip Carrier

Table 4 - Package Thermal Characteristics

PACKAGE TYPE	θ_{jc}	θ_{ja} Still air	θ_{ja} 300 ft/min.	UNITS
44-pin PLCC	15	52	40	°C/W

ORDERING INFORMATION

The SMAR FB1050 is available in a 44-pin Plastic Leaded Chip Carrier (PLCC) package. The following part number should be used to order the part.

PACKAGE TYPE	PART NUMBER
44-pin PLCC	SMAR FB1050

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CHAPTER I-B

Datasheets FB2050

PRELIMINARY INFORMATION

SMAR FB2050 FIELDBUS COMMUNICATION CONTROLLER

- Based on the ISA SP50-02-1992 Part 2, Fieldbus Physical layer Definition
- Provides Software Selectable Full and Half Duplex Communication
- Automatic Polarity Detection and Correction for Incoming Manchester Signal
- Software Controlled FCS Generation for Transmitter and Automatic FCS Detection for the receiver
- Compatible with Most Microprocessors and Microcontrollers with Special interface pins provided for M68HC11 controller
- RAM and PROM Paging and Chip-Select logic provided to reduce System Chip Count
- 31.25K Bits/Second Data Rate
- Low Power Consumption Typically 2 mA
- Available in 100-Pin PQFP Package
- Transmitter Jabber Inhibit Circuitry

The SMAR FB2050 is the second generation of SMAR's Fieldbus microcontrollers. It includes all the features provided by the SMAR FB1050 controller plus additional features to facilitate hardware and software design. More notable of these features include FCS generation and detection, software controlled chip-select pins for IO interface, memory management capabilities and additional interface logic for use with the M68HC11 microcontroller which is the choice microcontroller for the FB2050. Figure 1 shows the pin diagram of the FB2050.

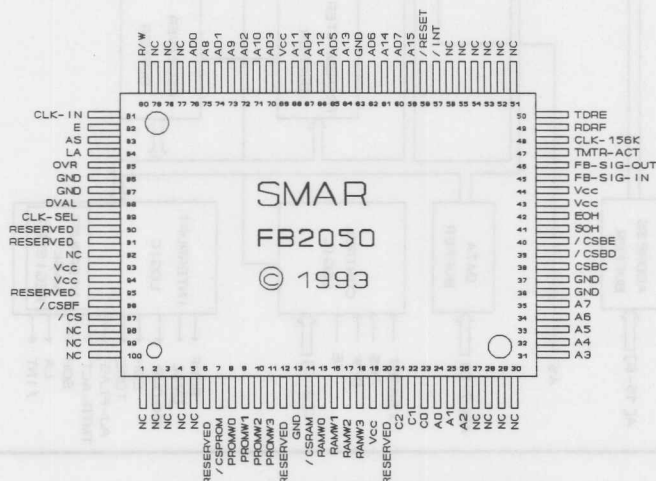


Figure 1 - FB2050 Pin Diagram

Figure 2 shows the block diagram of the FB2050:

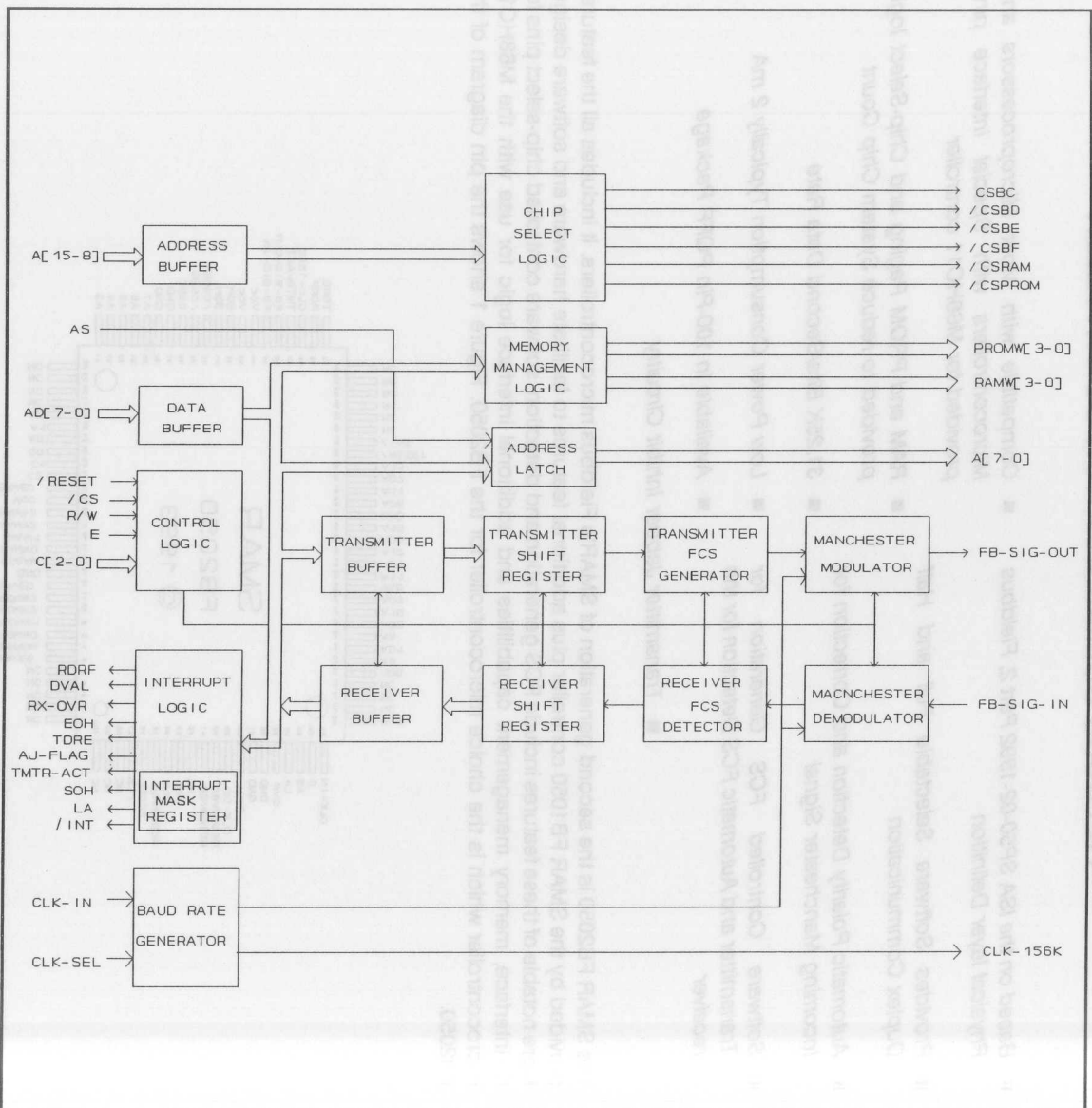


Figure 2 - FB2050 Block Diagram

PINOUT SUMMARY

Table 1 shows the pinout of the FB2050 with a brief pin description. Detailed functional description of each pin is presented following table 1.

Pin Number	Pin Name	Pin Type	Pin Description
7	/CSPROM	Output	Chip Select for External PROM
8-11	PROMW[0-3]	Output	PROM Page Selector Bus
14	/CSRAM	Output	Chip Select for External RAM
15-18	RAMW[0-3]	Output	RAM Page Selector Bus
21-23	C[2-0]	Input	Control Bus
24-26	A[0-2]	Output	Address Latch Output
31-35	A[3-7]	Output	Address Latch Output
38	CSBD	Output	Active High Chip-Select @ BCXX
39	/CSBD	Output	Active Low Chip-Select @ BDXX
40	/CSBE	Output	Active Low Chip-Select @ BEXX
41	SOH	Output	Start of Header Delimiter Indicator
42	EOH	Output	End of Header Delimiter Indicator
45	FB-SIG-IN	Input	Fieldbus Signal Input Pin
46	FB-SIG-OUT	Output	Fieldbus Signal Output Pin
47	TMTR-ACT	Output	Transmitter Activity Signal
48	CLK-156K	Output	Output Clock, 156.25 KHz
49	RDRF	Output	Receiver Data Register Full
50	TDRE	Output	Transmitter Data Register Empty
57	/INT	Output	Interrupt Request Signal
58	/RESET	Input	Master Reset
59, 61, 64, 66	A[15-12]	Input	Address Bus
68, 71, 73, 75	A[11-8]	Input	Address Bus
60, 62, 65, 67	AD[7-4]	Input/Output	Multiplexed Address/Data Bus
70, 72, 74, 76	AD[3-0]	Input/Output	Multiplexed Address/Data Bus
80	R/W	Input	Read/Write
81	CLK-IN	Input	Input Clock (625 KHz or 1.25 MHz)
82	E	Input	E Clock (From M68HC11)
83	AS	Input	Address Strobe (From M68HC11)
84	LA	Output	Receiver Activity
85	RX-OVR	Output	Receiver Overrun
88	DVAL	Output	Receiver Data Valid
89	CLK-SEL	Input	Clock Select
6, 12, 20, 90, 91, 95	RESERVED	-	-
96	/CSBF	Output	Active Low Chip Select @ BFXX
97	/CS	Input	/CS Signal
13, 36, 37, 63, 86, 87	GND	-	Ground
19, 43, 44, 69, 93, 94	Vcc	-	Supply Voltage +5V
1-5	Do Not Connect	-	-
27-30	Do Not Connect	-	-
51-56	Do Not Connect	-	-
77-79	Do Not Connect	-	-
92, 98, 99, 100	Do Not Connect	-	-

Table 1 - FB2050 Pins

PINS DESCRIPTION:

The pins of the FB2050 can be divided into five groups: microprocessor interface pins, chip-select pins, memory paging pins, receiver pins and transmitter pins.

the direction of data transfer between the FB2050 and the processor. A high signal on this pin indicates reading the FB2050. A low signal indicates writing to the FB2050.

MICROPROCESSOR INTERFACE PINS:

CLK-IN: Master Clock Input; all internal timing signals are derived from this clock. For low speed Fieldbus applications, the frequency of this clock must be 625KHz $\pm 0.2\%$ or 1.25 MHz $\pm 0.2\%$.

CLK-SEL: Input Clock Select; selects the CLK-IN frequency input.
High: 1.25 MHz **CLK-IN**
Low: 625 KHz **CLK-IN**

E: This input should be connected to the E clock of the M68HC11 controller. All read and write operations are synchronized with the positive cycle of this clock.

AS: This input should be connected to the **AS** output of the M68HC11. An active high pulse on this pin latches the low address bus, **AD[7-0]**, into the internal 8-bit latch. The outputs of this latch is connected to pins **A[7-0]**.

/CS: This pin should be connected to an active low pulse source synchronized with the other interface pins to provide pulses needed for read and write operations.

R/W: Read/Write; this pin indicates

/RESET:

Hardware Reset; a low pulse on this pin resets the entire chip.

C[2-0]:

Control Bus; these three lines are used to control all read and write operations of the FB2050 internal registers. Table 2 shows all pos-sible operations.

C2	C1	C0	R/W	Operation (synchronized with E)
0	0	0	0	TRANSMITTER_BUFFER
0	0	1	0	TRANSMITTER_RESET
0	1	0	0	START_TRANSMISSION
0	1	1	0	RECEIVER_RESET
1	0	0	0	INTERRUPT_MASK
1	0	1	0	CONTROL_REGISTER_1
1	1	0	0	PROM_PAGE_REGISTER
1	1	1	0	RAM_PAGE_REGISTER
X	0	0	1	RECEIVER_BUFFER
X	0	1	1	STATUS_REGISTER_1
X	1	0	1	INTERRUPT_STATUS
X	1	1	1	STATUS_REGISTER_2

Table 2: FB2050 Control Registers

AD[7-0]: Multiplexed address/data bus.

A[15-8]: High bits of address bus.

A[7-0]: These are the outputs of the internal address latch. The low address is latched with an active high pulse on **AS**. This internal latch eliminates the necessity for an external address latch.

/INT: Interrupt request; this signal goes low when an unmasked

internal interrupt source generates an interrupt request. The source of interrupt can be identified by reading the interrupt status register.

CHIP SELECT PINS:

/CSPROM: This pin provides an active low chip select pulse for the system PROM when the processor accesses address C000-FFFF or 4000-7FFF.

/CSRAM: This pin provides an active low chip select pulse for the system RAM when the processor accesses address 0200-3FFF or 8000-AFFF.

CSBC: This line creates an active high pulse when the processor accesses address BC00-BCFF.

/CSBD: This line creates an active low pulse when the processor accesses address BD00-BDFF.

/CSBE: This line creates an active low pulse when the processor accesses address BE00-BEFF.

/CSBF: This line creates an active low pulse when the processor accesses address BF00-BFFF. Note that this signal can be used to generate the /CS for the FB2050.

MEMORY PAGING PINS:

PROMW[3-0]: These pins are outputs of a register which contains the page address for the PROM and are

active during any access to memory page 4000-7FFF. When any other address is accessed, the output of these pins are zero.

RAMW[3-0]:

These pins are outputs of a register which contains the page address for the RAM and are active during any access to memory page 0200-3FFF. When any other address is accessed, the output of these pins is zero.

RECEIVER PINS:

FB-SIG-IN: Fieldbus Digital Input Pin; This is a CMOS level input. Proper filtering and level conversion is required for the Fieldbus line.

RDRF: Receiver data register full; this signal goes high when there is a valid byte in the receiver data register. It goes low when the processor reads the receiver data. This signal is one of the sources that causes the INT signal to go low and can also be used as an independent interrupt request line.

LA: Receiver line activity. This signal goes high when FB2050 detects any transitions on the receiver line and it remains high until the FB2050 detects the absence of activity for about 160 μ s on the line (5 Fieldbus bit times).

DVAL: this signal goes high after the start delimiter has successfully been received. It goes low if the FB2050 receives a missing transition (N+ or N-). This signal is one of the sources that

causes the **INT** signal to go low and can also be used as an independent interrupt request line.

RX-OVR:

Receiver Overrun Flag; this signal goes high when the processor fails to read the receiver data register and a new byte is received. This signal is one of the sources that causes the **INT** signal to go low and can also be used as an independent interrupt request line.

SOH:

Receiver Start of Header Delimiter; this signal goes high after successful detection of start delimiter and goes low when **LA** goes low.

EOH:

Receiver End of Header Delimiter; this signal goes high after successful detection of end delimiter and goes low when **LA** goes low. This signal is one of the sources that causes the **INT** signal to go low and can also be used as an independent interrupt request line.

TRANSMITTER PINS:**FB-SIG-OUT:**

Fieldbus Digital Output Pin. This is a CMOS output buffer during transmission and is tristate when the transmitter is idle.

TDRE:

Transmitter Data Register Empty; this signal goes high when the transmitter buffer is empty. It goes low when the transmitter data register is written into. This signal is one of the sources that causes the

INT signal to go low and can also be used as an independent interrupt request line.

TMTR-ACT:

Transmitter Activity; this signal is low when the transmitter is idle. It goes high as soon as the transmitter starts its activity and stays high until the end of the message.

CLK-156K:

156.25KHz Clock Output for general purpose application.

REGISTER DEFINITIONS:

As shown in table 2, control bus input pins **C[2-0]** controls all read and write operations for the **FB2050**. By connecting these pins to the output pins **A[2-0]** respectively, all these operations can be performed by simply accessing some specific addresses of the memory map. Also, by connecting the output pin **/CSBF** to the input pin **/CS** will connect the **FB2050** to the address page **BFXX** avoiding the necessity for external chip select components (however any of the other active low chip select outputs can also be selected for this purpose). Table 3 describes all **FB2050** internal register and their addresses:

Register	Address BFXX + C[2-0]	Operation
TRANSMITTER_BUFFER	BF00	write only
TRANSMITTER_RESET	BF01	write only
START_TRANSMISSION	BF02	write only
RECEIVER_RESET	BF03	write only
INTERRUPT_MASK	BF04	write only
CONTROL_REGISTER_1	BF05	write only
PROM_PAGE_REGISTER	BF06	write only
RAM_PAGE_REGISTER	BF07	write only
RECEIVER_BUFFER	BF00	read only
STATUS_REGISTER_1	BF01	read only
INTERRUPT_STATUS	BF02	read only
STATUS_REGISTER_2	BF03	read only

Table 3 - FB2050 Internal Registers

TRANSMITTER_BUFFER: When The FB2050 transmitter is on, writing to address **BF00** transfers the byte on the data bus, **AD[7-0]**, into the transmitter data register. To avoid transmitter overrun, the **TDRE** flag inside the **STATUS_REGISTER_1** should be checked prior to a transmitter write operation to make sure that the transmitter is ready to receive the next byte to be transmitted.

TRANSMITTER_RESET: This reset operation has the same effect as hardware reset on the transmitter.

The receiver module and the chip select module are not affected by this operation.

START_Transmission: A write to this address forces the FB2050 transmitter out of the idle

state. The value of the data bus during this write is irrelevant. After the transmitter is turned on, it immediately starts to transmit a 16-bit preamble; followed by the **SOH**; and by the byte stored in the transmitter data register. In half duplex mode, the transmitter checks the status of the Field Bus Line before granting a start of transmission.

IMPORTANT: You must write the first byte of your message immediately after issuing a **START_Transmission**.

RECEIVER_RESET: This reset operation has the same effect as hardware reset on the receiver. The transmitter module and the chip select module are not affected by this operation.

INTERRUPT_MASK: This register is used to enable or disable the interrupt source generated by the FB2050. During **RESET** this register is cleared.

Figure 3 shows the interrupt mask register.

7	6	5	4	3	2	1	0
RDRF	DVAL	RX-FCS	EOH	RX-OVR	DPLL-LOCK	TMTR-ACT	TDRE
RESET: 0	0	0	0	0	0	0	0

Figure 3 - Interrupt Mask Register

TDRE: Interrupt on transmitter data register empty. It indicates that data may be written into the transmitter data register.

0 = Disable
1 = Enable

TMTR-ACT: interrupt on end of transmission. It indicates that entire transmission frame has ended and the Fieldbus line is free.

0 = Disable
1 = Enable

DPLL-LOCK: interrupt on the end of Manchester phase locked loop. It indicates that a valid frame has ended. The **DPLL-LOCK** internal signal goes high when the FB2050 detects a valid

Fieldbus Manchester signal and it remains high until the FB2050 detects 6 missing transition on the line. The falling edge of this internal signal causes an interrupt signal to CPU

0 = Disable

1 = Enable

RX-OVR: interrupt on receiver overrun. The receiver has detected an overrun error.

0 = Disable

1 = Enable

EOH: interrupt on successful detection of end of header delimiter. It indicates end of reception of one Fieldbus Message.

0 = Disable

1 = Enable

RX-FCS: Interrupt on receiver **FCS** detection. It indicates that the **FCS** calculated for the received frame is correct.

0 = Disable

1 = Enable

DVAL: Interrupt on detection of start of header delimiter. It indicates that the start delimiter was detected and that the following Manchester signal is a valid Fieldbus data.

0 = Disable

1 = Enable

RDRF: Interrupt on receiver data register empty. It indicates that the receiver data buffer contains a new valid byte.

0 = Disable

1 = Enable

CONTROL_REGISTER_1:

This register controls the basic operations for the FB2050 transmitter and receiver modules. During RESET this register is cleared.

Figure 4 shows this register:

7	6	5	4	3	2	1	0
X	X	X	X	FCS	H/F	EFC	X
RESET: 0	0	0	0	0	0	0	0

Figure 4 - CONTROL_REGISTER_1

EFC: Enable/Disable Fieldbus Communication System
(Transmitter, Receiver and Baud Rate Generator Modules)

0 = Disable

1 = Enable

FCS: Transmitter checksum generator

0 = Disable

1 = Enable

H/F: Half/Full duplex function selector

0 = Half duplex

1 = Full duplex

PROM_PAGE_REGISTER:

The PROM page register is a 4-bit register that contains the PROM page number used to extend the PROM address space. The value of this register is placed in the pins PROMW[3-0] only when the processor accesses the memory page **4000-7FFF**. When any other memory address is accessed PROMW[3-0] point to # 0. The user should never write the value 0 into this register. During RESET this register is set to # 1.

Figure 5 shows this register.

7	6	5	4	3	2	1	0
X	X	X	X	PROMW3	PROMW2	PROMW1	PROMW0
RESET: 0	0	0	0	0	0	0	1

Figure 5 - PROM_PAGE_REGISTER**RAM_PAGE_REGISTER:**

The RAM page register is a 4-bit register that contains the RAM page number used to extend the RAM address space. The value of this register is placed in the pins RAMW[3-0] only when the processor accesses the memory page **0200-3FFF**. When any other memory address is accessed RAMW[3-0] point to # 0. The user should never write the value 0 into this register. During RESET this register is set to # 1.

Figure 6 shows this register.

7	6	5	4	3	2	1	0
X	X	X	X	RAMW3	RAMW2	RAMW1	RAMW0
RESET: 0	0	0	0	0	0	0	1

Figure 6 - RAM_PAGE_REGISTER

RECEIVER_BUFFER:

The receiver data register can be read by accessing address BF00 .

STATUS_REGISTER_1:

This register contains all possible sources of interrupt available in the FB2050, it is located at the address BF01. This register is recommended for polling operations. After a RESET all flags will be cleared.

Figure 7 describes this register.

7	6	5	4	3	2	1	0
RDRF	DVAL	RX-FCS	EOH	RX-OVR	DPLL-LOCK	TMTR-ACT	TDRE
RESET: 0	0	0	0	0	0	0	0

Figure 7 - STATUS_REGISTER_1

INTERRUPT_STATUS:

The source of the interrupt is registered at this location. This register works in conjunction with the INTERRUPT_MASK and STATUS_REGISTER_1, if a source of interrupt is masked, its corresponding bit in the INTERRUPT_STATUS register will be 0. This register is cleared immediately after a read operation is performed, so its value should be stored in memory until all interrupt sources are properly processed. During RESET all these flags will be cleared.

Figure 8 describes the contents of this register.

IMPORTANT: Never use INTERRUPT_STATUS for polling procedures, STATUS_REGISTER_1 should be used for these type of applications.

7	6	5	4	3	2	1	0
RDRF	DVAL	RX-FCS	EOH	RX-OVR	DPLL-LOCK	TMTR-ACT	TDRE
RESET: 0	0	0	0	0	0	0	0

Figure 8 - INTERRUPT_STATUS register

STATUS_REGISTER_2:

This register contains some additional status information for the receiver and transmitter modules of the FB2050. During reset its values are cleared.

Figure 9 describes the contents of this register.

7	6	5	4	3	2	1	0
1	AJ-FLAG	POLARITY	LA	1	TXS2	TXS1	TXS0
RESET: 0	0	0	0	0	0	0	0

Figure 9 - STATUS_REGISTER_2

AJ-FLAG: Anti Jabber flag. It signals a transmitter error when the FB2050 has been using the transmission line for more than 131 ms (512 Fieldbus byte times).

POLARITY: Indicates the polarity of the received Fieldbus signal
1 = Negative polarity
0 = Positive polarity

LA: Line Activity
1 = Line is busy
0 = Line is free

TXS2-TXS0: Transmitter State
These bits indicate the state of the transmitter submodule. Table 4 describe all these states.

TXS 2	TXS 1	TXS 0	Transmitter State
0	0	0	Idle
0	0	1	Send Preamble
0	1	0	Send Preamble
0	1	1	Send SOH
1	0	0	Send Data
1	0	1	Send FCS High
1	1	0	Send FCS Low
1	1	1	Send EOH

Table 4 - STATUS_REGISTER_2 versus Transmitter states

BASIC OPERATING PROCEDURES:**STARTUP PROCEDURE:**

- 1- Apply a low level hardware reset immediately after powerup.
- 2- Program desired values for CONTROL_REGISTER_1.
- 3- Program the desired value INTERRUPT_MASK.
- 4- Program the desired values for RAM_PAGE_NUMBER and PROM_PAGE_NUMBER if applicable.

is not applicable you must:

- 1- Write a dummy value into TRANSMIT-TER_RESET.
- 2- Recover all values for CONTROL_REGISTER_1.
- 3- Recover all values for INTERRUPT_MASK.
- 4- Perform normal operations for the transmitter submodule.

TRANSMITTER SUBMODULE:

The following paragraphs describe the necessary steps that should be followed for a successful Fieldbus Transmission Frame:

- 1- Turn the transmitter on (dummy write to START_TRANSMISSION).
- 2- Write the first byte into the TRANSMITTER_BUFFER register.
- 3- Enable the processor's interrupt or polling system on TDRE.
- 4- Write the next byte of the message every time TDRE is high.
- 5- Finish the message by allowing a transmitter underrun. In this situation, the FB2050 will send the FCS (if enabled) followed by the EOH and enters the idle state.

If an anti jabber error has occurred the transmitter will be locked into the idle state until a hardware or software reset is performed. If hardware reset

RECEIVER SUBMODULE:

The following steps describes the normal operation for the FB2050 Receiver Submodule:

- 1- Enable the processor's interrupt or polling system on RDRF.
- 2- Read the RECEIVER_BUFFER register every time RDRF is high.
- 3- If the received message contains an FCS, check the interrupt status register to make sure the FCS was correctly detected.

If a receiver overrun error has occurred it is very important that the software recognizes this occurrence and provide a proper reset sequence to the chip. The following steps should be performed.

- 1- Wait until STATUS_REGISTER_2 signals LA = 0.
- 2- Write a dummy value into RECEIVER_RESET.

- 3- Recover all values for CONTROL_REGISTER_1. memory capacity to 248 Kbytes.
- 4- Recover all values for INTERRUPT_MASK. If any other address is accessed these pins will vector to page #0.
- 5- Perform all normal operations for the Receiver Submodule. To assure non paged operation compatibility the register RAM_PAGE_NUMBER is set to #1 during hardware RESET.

CHIP SELECT AND MEMORY MANAGEMENT:

The chip select logic is specially designed to interface with the Motorola M68HC11 memory definitions, but others Microprocessors could be used as well. Figure 10 shows the memory map implemented by the FB2050 chip select logic.

0000	Reserved
0200	15872 B RAM PAGED
4000	16K PROM PAGED
8000	12K High RAM
8000	8000 to BBF is reserved for internal registers BC00, /BD00, /BE00, /BF00
C000	16K High PROM
FFFF	

Figure 10 - Memory Map Implemented by FB2050

/CSRAM pin provides an active low pulse when the processor access the space reserved for RAM from 0200 to 3FFF or 8000 to AFFF.

During any access from 0200 to 3FFF, the pins RAMW[3-0] will vector the contents of the FB2050 register RAM_PAGE_NUMBER providing an extended address space for the RAM memory employed. This process will extent the RAM

/CSPROM pin provides an active low pulse when the processor access the space reserved for PROM from 4000 to 73FFF or C000 to FFFF.

During any access from 4000 to 7FFF, the pins PROMW[3-0] will vector the contents of the FB2050 register PROM_PAGE_NUMBER providing an extended address space for the PROM memory employed. This process will extent the PROM memory capacity to 256K bytes.

If any other address is accessed these pins will vector to page #0.

To assure non paged operation compatibility the register PROM_PAGE_NUMBER is set to #1 during hardware RESET.

RECOMMENDED OPERATING CONDITIONS

Temperature Range	Power Supply Tolerance
-20 to +70° C	±5% of V _{cc}

Table 5 - Recommended Operating Conditions

ABSOLUTE MAXIMUM RATINGS

V _{cc}	DC Supply Voltage	-0.5 to +7.0 V
V _{in}	Input Voltage	-0.5 to V _{cc} + 0.5 V
V _o	Output Voltage	-0.5 to V _{cc} + 0.5 V
I _{ik}	Input Clamp Current	±20 mA
I _{ok}	Output Clamp Current	±20 mA
I _{ok}	Continuous Output Current	±25 mA
T _{STG}	Storage Temperature	-65 to +150° C

Table 6 - Absolute Maximum Ratings

PACKAGE THERMAL CHARACTERISTICS

Pin Count	θ_{jc}	θ_{ja} (Still Air)	θ_{ja} (300 ft/m)
100	13° C/W	55° C/W	47° C/W

Table 7 - Package Thermal Characteristics

θ_{jc} is the junction to case thermal characteristics and θ_{ja} is the junction to ambient air characteristics.

ELECTRICAL SPECIFICATIONS

Parameter	Min	Max
V_{OH}	3.84 V	-
V_{OL}	-	0.33 V
V_L	-0.30 V	0.80 V
V_H	2.00 V	$V_{CC} + 0.3$ V
Input Transition Time	-	500 nS
I/O Capacitance	-	10 pF
Standby Current	-	10 mA
Leakage Current	-10 μ A	10 μ A
Output Short Circuit Current ($V_o = V_{CC}$)	20 mA	140 mA
Output Short Circuit Current ($V_o = V_{CC}$)	-10 mA	-100 mA

Table 8 - Electrical Specification

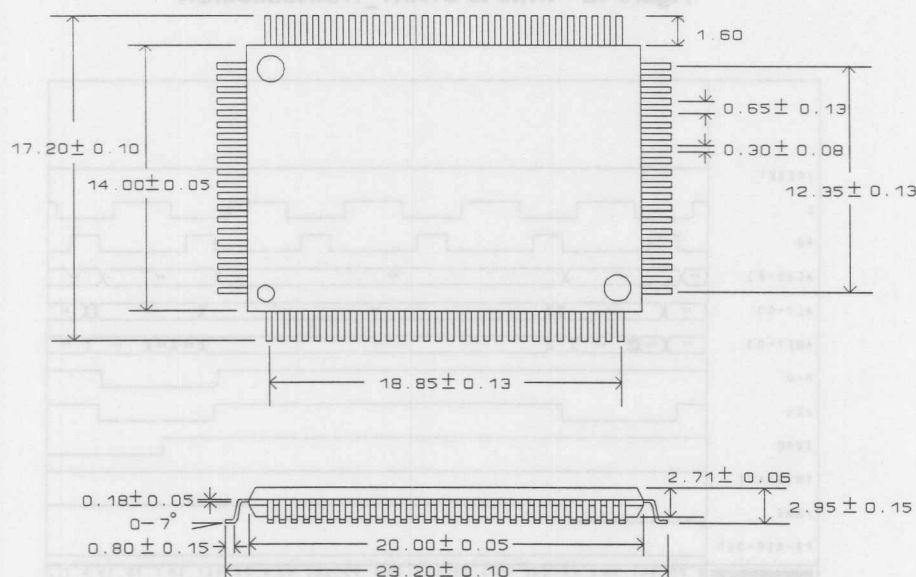
MECHANICAL SPECIFICATIONS

Figure 11 - Mechanical Specification

TIMING DIAGRAMS

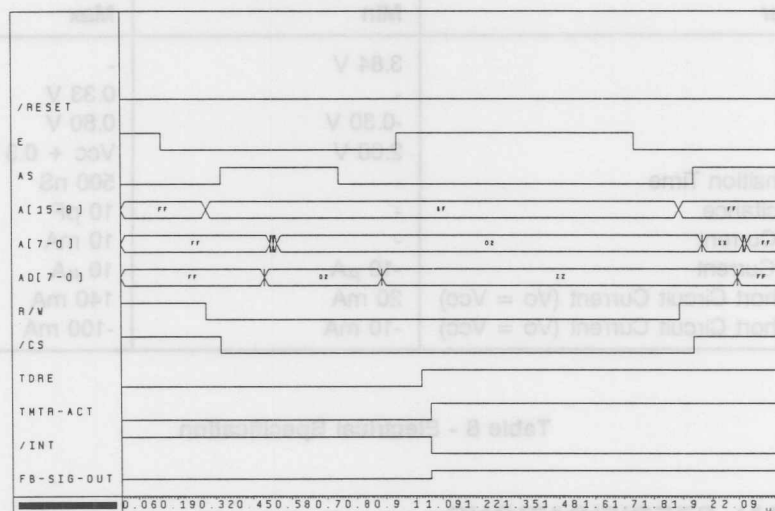


Figure 12 - Write to START_TRANSMISSION

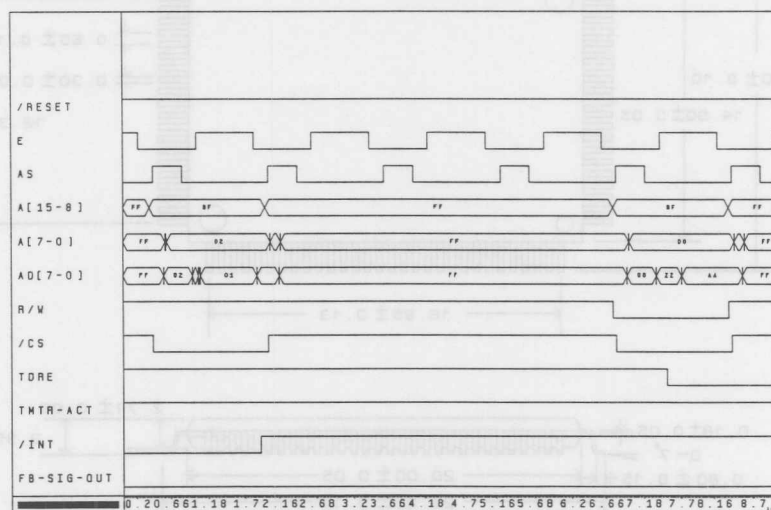


Figure 13 - Read INTERRUPT_STATUS and Write (AA) to TRANSMITTER_BUFFER

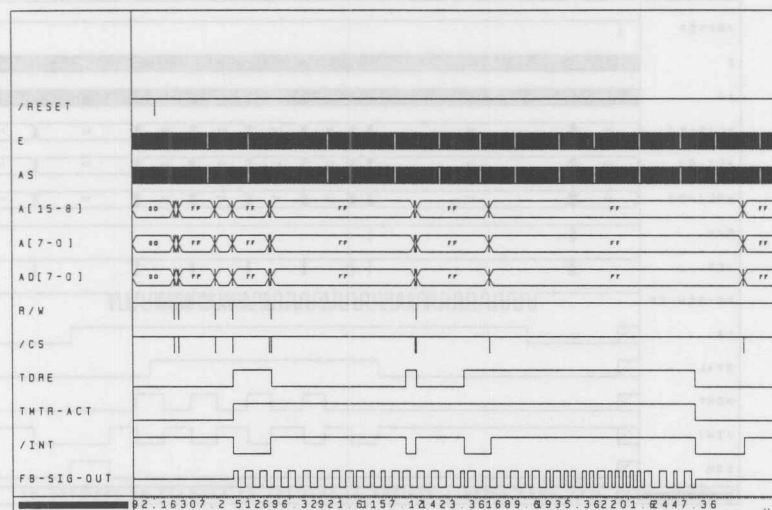


Figure 14 - Typical Transmission Procedure: 2 Bytes + FCS

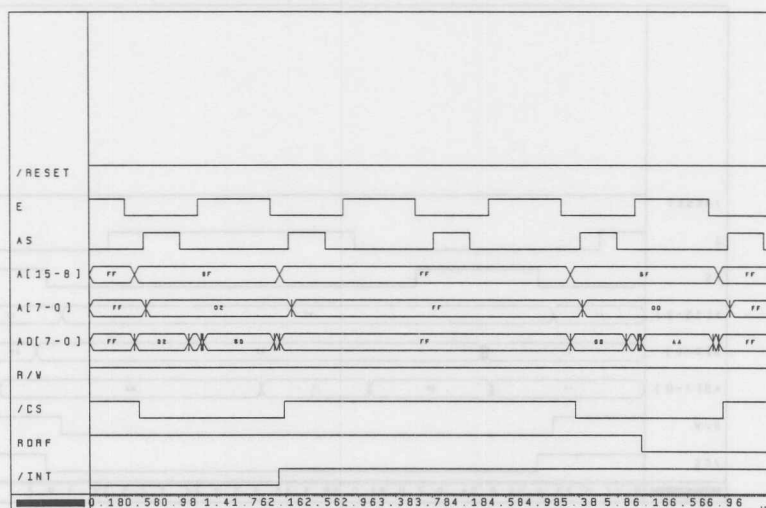


Figure 15 - Read INTERRUPT_STATUS Followed by Read RECEIVER_BUFFER

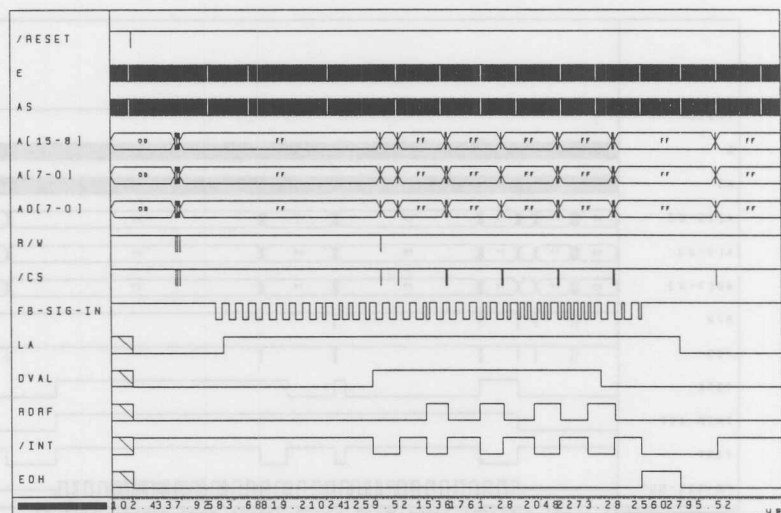


Figure 16 - Typical Reception Procedure: 2 Bytes + FCS

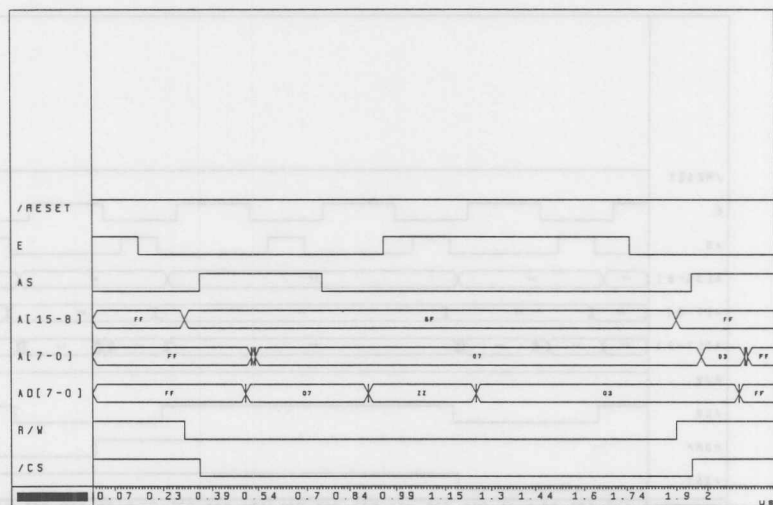


Figure 17 - Write (#03) to RAM_PAGE_REGISTER

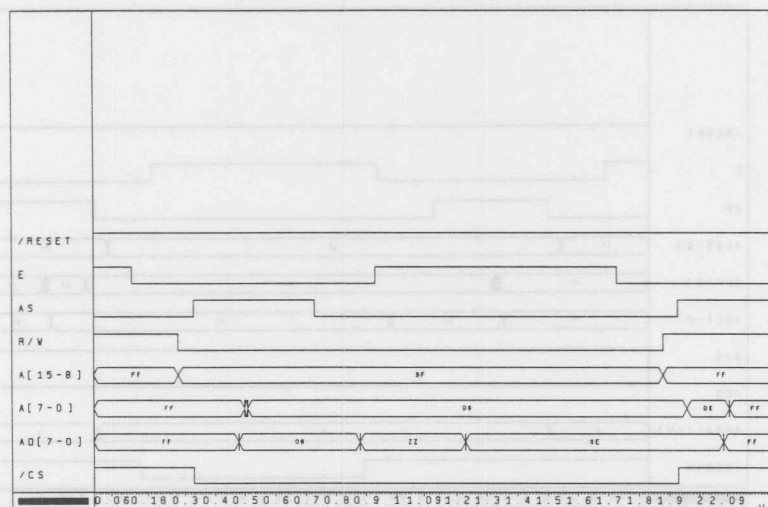


Figure 18 - Write (#0E) to PROM_PAGE_REGISTER

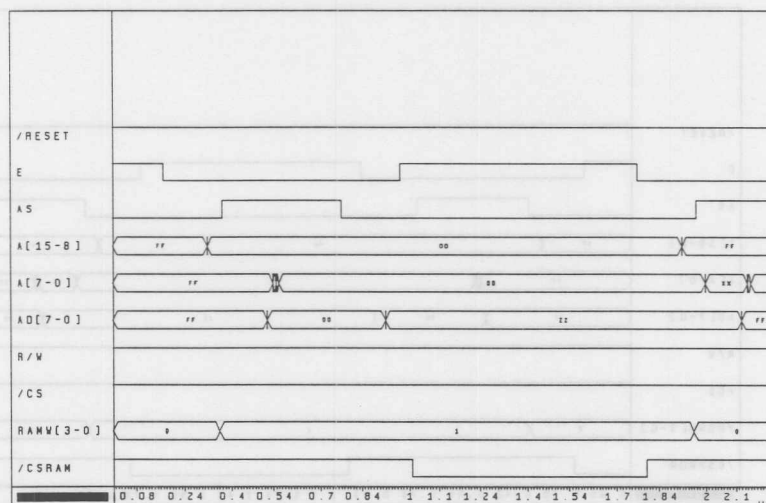


Figure 19 - Typical Read Operation from RAM Page #1

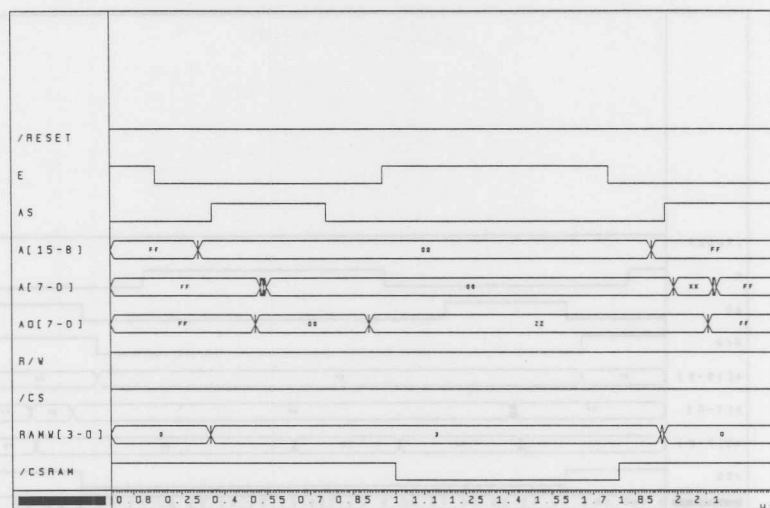


Figure 20 - Typical Read Operation from RAM Page #3

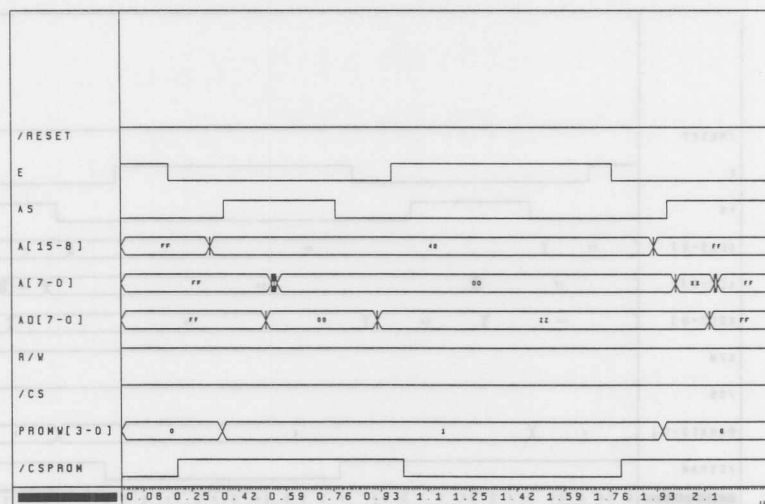


Figure 21 - Typical Read Operation from PROM Page #1

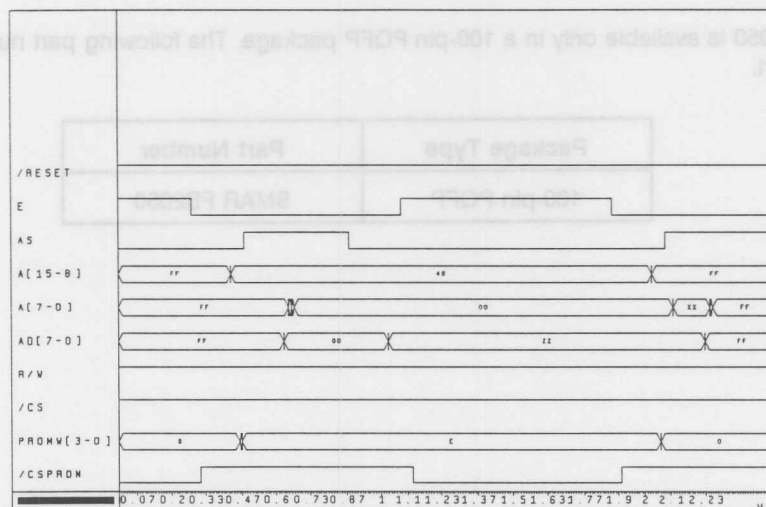


Figure 22 - Typical Read Operation from PROM Page #E

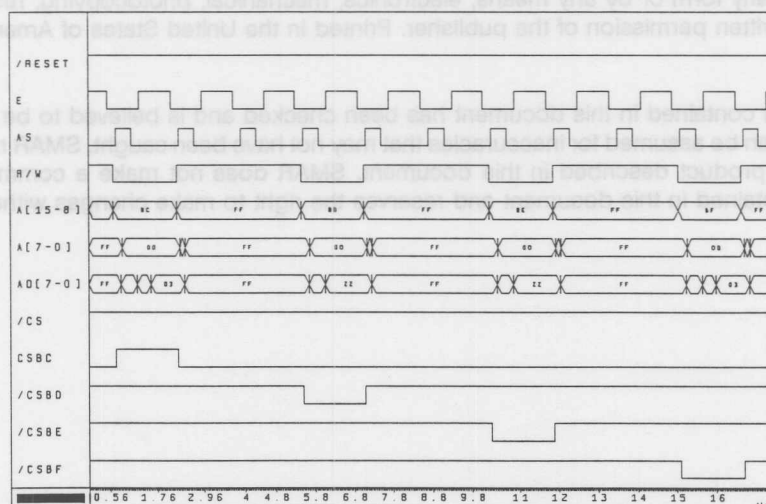


Figure 23 - Typical I/O Chip Selects

ORDERING INFORMATION

The SMAR FB2050 is available only in a 100-pin PQFP package. The following part number should be used to order the part.

Package Type	Part Number
100-pin PQFP	SMAR FB2050

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CHAPTER I-C

Datasheets FB3050

PRELIMINARY INFORMATION

SMAR FB3050 FIELDBUS COMMUNICATION CONTROLLER

- Based on the ISA SP50-02-1992 Part 2, Fieldbus Physical layer Definition
- Provides Software Selectable Full and Half Duplex Communication
- Automatic Polarity Detection and Correction for Incoming Manchester Signal
- Software Controlled FCS Generation for Transmitter and Automatic FCS Detection for the receiver
- Dual Channel Direct Memory Access
- Transmitter Jabber Inhibit Circuitry
- Compatible with Most Microprocessors and Microcontrollers with Special interface pins Provided for M68HC11 controller
- RAM and PROM Paging and Chip-Select logic provided to reduce System Chip Count
- 31.25K Bits/Second Data Rate
- Low Power Consumption Typically 2 mA
- Available in 144-Pin PQFP Package
- Multi Entry Fieldbus Address Recognition

SMAR FB3050 is the third generation of SMAR's Fieldbus microcontrollers. It includes all the features to facilitate hardware and software design. More notable of these features include dual channel DMA interface so the system can receive or transmit full messages with no CPU assistance. Also, included is a Fieldbus address recognition system that will signal the CPU if the message being received is addressed to a local node. Figure 1 shows the pin diagram of the FB3050.

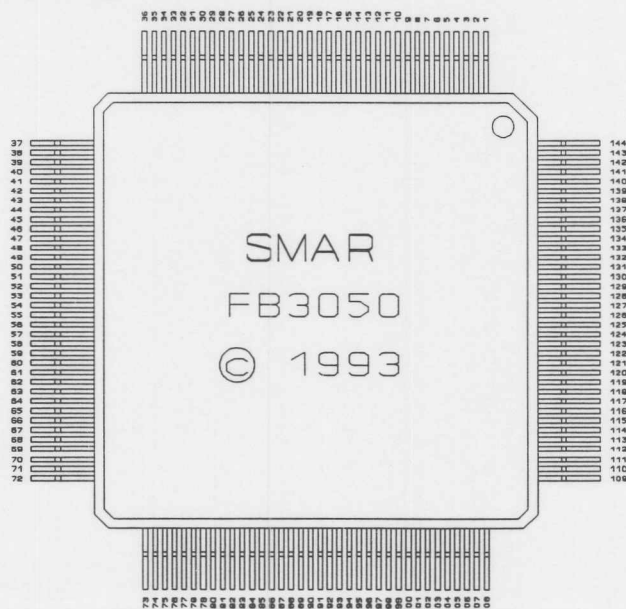


Figure 1 - FB3050Pin Diagram

CHAPTER II

Application Notes FB1050

PRELIMINARY INFORMATION

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INTRODUCTION

This Application Note will lead you to a successful hardware implementation of a generic field bus device.

It contains important information and complements the FB1050 Data Sheet. Before using this Application Note become familiar with the FB1050 Data Sheet.

This document provides working knowledge to implement data transmission and reception routines for the FB1050 in a Fieldbus environment. All procedures recommended here for this environment are for illustrative purposes only and are based on our best knowledge of the information available today. As the "Link Layer Protocol for Fieldbus" becomes available Smar Research will study all the possibilities for publishing a more complete review of this document. The user should analyze and understand all Figures of this Application Note before proceeding.

HARDWARE APPLICATION NOTES

This section contains additional information for FB1050 specifications, and some considerations about the interface circuitry that usually are required for a full field bus system. It compiles knowledge of the FB1050 and also our experience in the design of low power electronic instruments. The user should be familiar with the electronic diagrams found on Figures 4,5 & 6 for a proper understanding of this section.

POWER SUPPLY CONSIDERATIONS

The internal die of the FB1050 requires 5 pads connected to VCC and 5 pads connected to ground. These 5 pins should be externally interconnected with tracks as short as possible. Long loops must be avoided. One 100NF monolithic

type decoupling capacitor should be placed as close as possible to these power pins.

Normal operation is guaranteed for VCC voltages from 4.5 to 5.5 Volts. There are successful tests for voltages down to 3.3 Volt under special circumstances. Voltages below 3 Volt must be avoided because the internal CMOS drivers could enter into an invalid state resulting an increased power supply current ICC. To avoid a higher than normal ICC during the power-up stage, VCC should go from 0 to the 5 Volt level in less than 20 msec.

DIGITAL INPUT AND OUTPUT PINS

The FB1050 is made with CMOS technology and all signal pins are CMOS voltage levels compatible. For minimum power dissipation, all inputs should be driven as close as possible to VCC or GND ($\pm 0.1V$), and all outputs should drive low capacitance CMOS loads only. Fan out capabilities are estimated to be 4 LSTTL loads; if more loads are required, an external buffer should be used.

Integrated circuits can be damaged by exposure to illegal voltages or conditions. ZAP and LATCHUP are terms familiar to failure analysis on CMOS devices. You must provide proper Antistatic protection and never apply any voltage above VCC or below GND to the pins of this circuit. Avoid the use of separate power sources on the circuitry interfacing the FB1050.

Clk_In 625KHZ

This input is the time base for all internal circuitry. The accuracy of the internal baud rate generator for 31.25Kbps is dependent on this input frequency. This frequency must be stable and accurate to $\pm 0.2\%$ as per the requirements of the ISA-SP50.02-

FUNCTIONAL DESCRIPTION

GENERAL

The SMAR FB1050 is a synchronous transmitter/receiver communication controller designed to be interfaced with most common microprocessors and microcontrollers. It is based on the ISA-S50.02-1992-Part 2 Fieldbus physical layer definition. In this communication environment, parallel data is converted to serial and is transmitted using Manchester encoding. Received data is converted from Manchester code into 8-bit parallel bytes and presented to the CPU. With the SMAR FB1050, the conversion process, as well as all other operations of the chip, is totally transparent to the CPU. The CPU regards the FB1050 as an I/O port. Table 1 contains the signal names, type, pin number and pin description of the FB1050 chip. Following is a more detailed description of the pin signals.

GENERAL SIGNALS:

DO through D7 (Data Bus Buffer)

This is an 8-bit, bidirectional buffer used to interface the SMAR FB1050 to the CPU bus. The data received in the receiver buffer is passed onto the processor via these lines. The CPU data are passed onto the transmitter via these same lines.

Reset (Active Low Reset)

When the reset line is pulled low by the CPU, the chip enters an idle state and stays in that state for as long as the reset pin is low.

A minimum pulse duration of 200 ns is required to force the chip into idle state.

CLK (Clock)

The clock generates internal timing signals. For proper operation, the frequency of the clock must be at 20 times the data rate desired. For low speed Fieldbus application, CLK = 625 KHz.

RXRD (Receiver Read Data)

With low on this input signal, the FB1050 will write the contents in the receiver buffer into the data bus.

TXWR (Transmitter Write)

With low on this input signal, the FB1050 will write the contents in the data bus into the transmitter buffer.

SIG-OUT (Transmitter Fieldbus Signal Out)

This is the transmitter's modem digital output signal. During the idle state, this output is high impedance. This output should be connected to Media Attachment Unit (MAU) which is a wave shaping filter and a current (or voltage) modulator attached to the transmission media or the Fieldbus lines.

SIG-IN (Receiver Fieldbus Signal In)

This is the digital input connected to the receiver demodulator. This pin should be connected to the Media Attachment Unit which is an input filter connected to an analog comparator.

FB1050 PIN NAME	PIN DESCRIPTION	HC11 PIN DESCRIPTION
LA	Line Activity	Peripheral port; input.
/TXON	Transmitter On	Peripheral port; output.
/TXWR	Transmitter Write	Chip Select Write @ \$6000
TDRE	Transmitter Data Reg Empty	Transmitter Interrupt
D7-D0	Data lines D7 - D0	Data Bus
Sig_Out	Modulator Output	Connected to Output Filter

Table 1 - Pins Description

DATA TRANSMISSION SOFTWARE CONSIDERATIONS

A successful Token Pass Network will avoid more than one node transmitting at a given time, so Line Activity (LA) must be low before a Transmitter On (/TXON) is asserted.

The user software should check LA before starting a data transmission, ensuring the "Link Layer" procedures that there is not a multiple access in the Fieldbus line. It is also helpful to maintain active the receiver routines so the user software can check the message sent versus the message received to detect any loss of information.

Data transmission is accomplished by activating the Modulator (strobing /TXON), followed by consecutive data Write (/TXWR) into the Transmitter Data Buffer. These sequential writes must be synchronized with Transmitter Data Register Empty TDRE high.

The FB1050 does not implement the CHECK SUM calculation, thus the microprocessor must perform

all calculations and then Write the value into the Transmitter Buffer before terminating the transmission. The 16 bits CHECK SUM value will be considered as 2 additional bytes of the message.

The FB1050 will perform an automatic End of Message procedure after the processor stops writing data into its Transmitter Buffer.

The following pseudo code represents a data transmission procedure.

INITIALIZATION: (Needs to be done only once at power-up.)

Configuration of peripheral ports and chip select lines.

END INITIALIZATION.

TRANSMIT_MESSAGE:

IF LA != 0 Inform Link Layer of multiple access.

/TXON = 0 minimum 200 nS.

/TXON = 1 forever.

WRITE 1st BYTE_OF_MESSAGE.

TDRE Interrupt driven routine

DO WRITE Nnt BYTE_OF_MESSAGE.

UNTIL Transmit Data Buffer is empty.

END TRANSMIT_MESSAGE:

DATA RECEPTION HARDWARE CONSIDERATIONS

This section contains information for FB1050 data reception. The communication controller will resolve

Modulator Control Pins:

TXON (Transmitter On)

This active low input signal drives the FB1050 from idle state into the transmission state. When TXON goes high, the SIG-OUT sends an 8 to 15-bit preamble, followed by the start delimiter. Then the data is written into the transmitter buffer. On the negative edge of TXON, RTS goes high. After the rising edge of TXON, a transmitter buffer write is recommended; this should be done before the end of the preamble transmission.

RTS (Transmitter Request To Send)

This output signal goes high on the falling edge of TXON and remains high until the last bit of the message is sent. It goes low when the transmission is complete.

CTS (Clear To Send)

When the first bit of the data is transmitted, this output data goes high. Note that preambles and delimiters are not considered to be part of the data. CTS goes low as soon as the last bit of data is transmitted.

TDRE (Transmitter Data Register Empty Flag)

This flag goes high when the transmitter data register is empty. The transmitter data register is empty when data is transferred from the transmitter buffer into the transmitter shift register. This is done automatically. TDRE goes low when this transfer takes place. TDRE can be used as a transmitter interrupt request or as a general purpose polling line. If the CPU fails to write to 14 transmitter data register within 8 bits of time space, the modulator will underrun and start the end-of-message procedure.

Demodulator Control Pins:

LA (Receiver Line Activity)

This output pin signals Fieldbus activity on the line. It goes high when a high-to-low transition followed by a low-to-high transition is detected on

the line. It goes low after six missing transitions are detected on the SIG-IN line.

OVR (Receiver Overrun Flag)

This flag goes high when the demodulator detects a byte was lost by the CPU.

DVAL (Receiver Data Valid Flag)

This flag goes high after successful reception of Start Delimiter. It goes low after the first missing Manchester symbol (N+ or N-). For successful communication this missing Manchester symbol should be part of the end delimiter character.

RDRF (Receiver Data Register Full Flag)

This flag goes high to indicate the transfer of a valid byte between the receiver shift register and the receiver buffer. It goes low when the RXRD signal goes low. RDRF can be used as an interrupt request line to signal the CPU to start reading the received byte.

To perform the Analog Loop-Back test, simply connect the terminals of your instrument into a Fieldbus line, activate the transmit and receive routines. The data transmitted onto the fieldbus line should be read by the receive routine.

This test will confirm the proper operation of the entire system.

Since this test affects the Fieldbus line, the test message must conform to the Link Layer Protocol in use.

TIMING DIAGRAMS

This section will illustrate the timing considerations for the SMAR FB1050 and guide the reader through the timing diagrams.

/RESET TIMING CONSIDERATIONS

The /RESET pulse is required to be a minimum of 200 nsec. Figures 1 and 2 have an extended reset pulse to show the logic definition of all output pins of the FB1050.

After /RESET is released all these outputs will remain at the "reset state" until there is a disturbance in this state.

This disturbance can be a result of receiving a valid Preamble sequence of 2 Manchester bits from the Fieldbus line (LA goes high), or by activating /TXON causing the FB1050 to start transmitting a Preamble of a message.

/RESET must be applied during power-up to guarantee the Modulator and the Demodulator into a known state. The FB1050 should be reset only once.

/TXON AND /TXWR TIMING CONSIDERATIONS

Refer to the timing diagram of Figure 1.

The FB1050 allows the transmitter Modulator to be turned on any time after reset. However, after the Modulator is turned on, the microprocessor should write into the Transmitter Buffer no later than 512 usec.

If the user software fails to write within this time the Modulator will send the invalid contents of the Transmitter Buffer.

We recommend the first byte of the message to be written immediately after the pin /TXON returns high.

/TXWR AND TDRE TIMING CONSIDERATIONS

Refer to the timing diagram on Figure 1.

The Transmitter Modulator will raise the TDRE pin as soon the data contained in the Transmitter Buffer is transferred into the Transmitter Shift Register.

TDRE goes low after the microprocessor writes into the Transmitter Buffer.

If a transfer between the Transmitter Buffer and the Transmitter Shift Register is performed while TDRE is still high, the Modulator will start to send the End Delimiter sequence and then enter into the reset state. Once in reset state, only /TXON will enable the Modulator. The maximum time between TDRE going high and /TXWR going low should be less than 256usec, otherwise the FB1050 will enter the End of Message procedure.

LA, DVAL AND POL TIMING CONSIDERATIONS

Refer to the timing diagram of Figure 2.

LA will be cleared during reset and will remain in this

TIMING DIAGRAMS

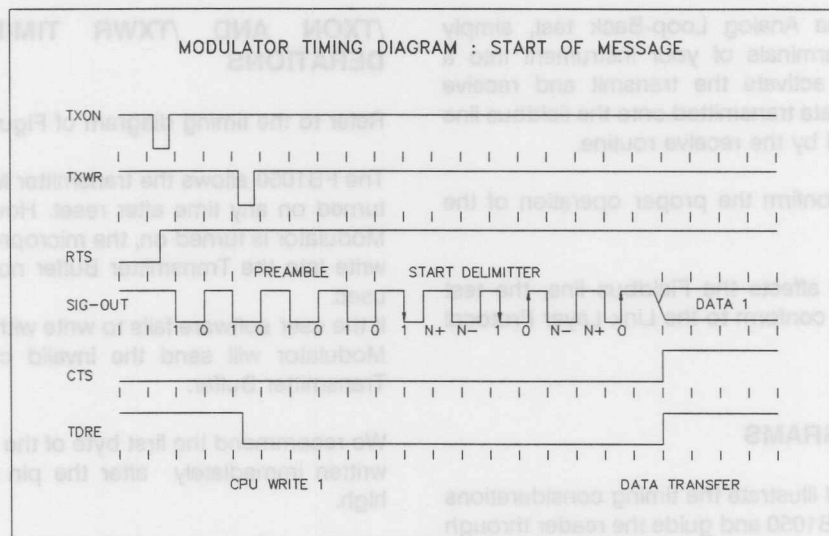


Figure 4 - Modulator Timing Diagram; Start of Message

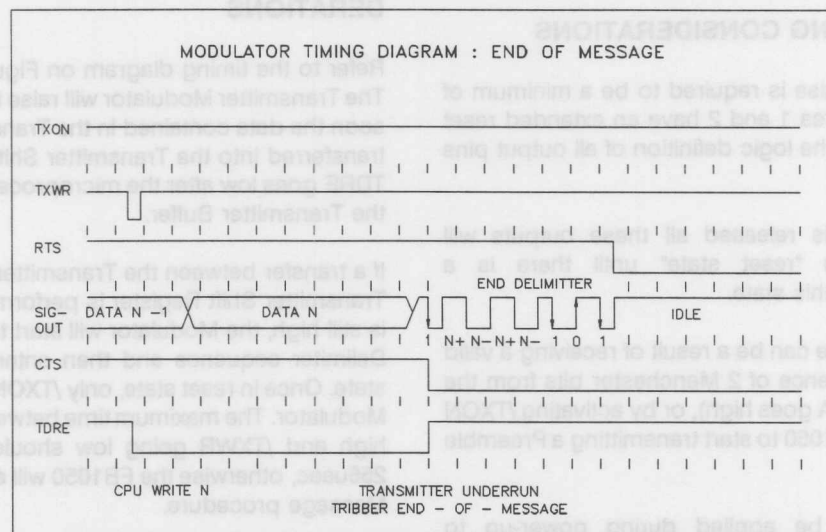


Figure 5 - Modulator Timing Diagram; End of Message

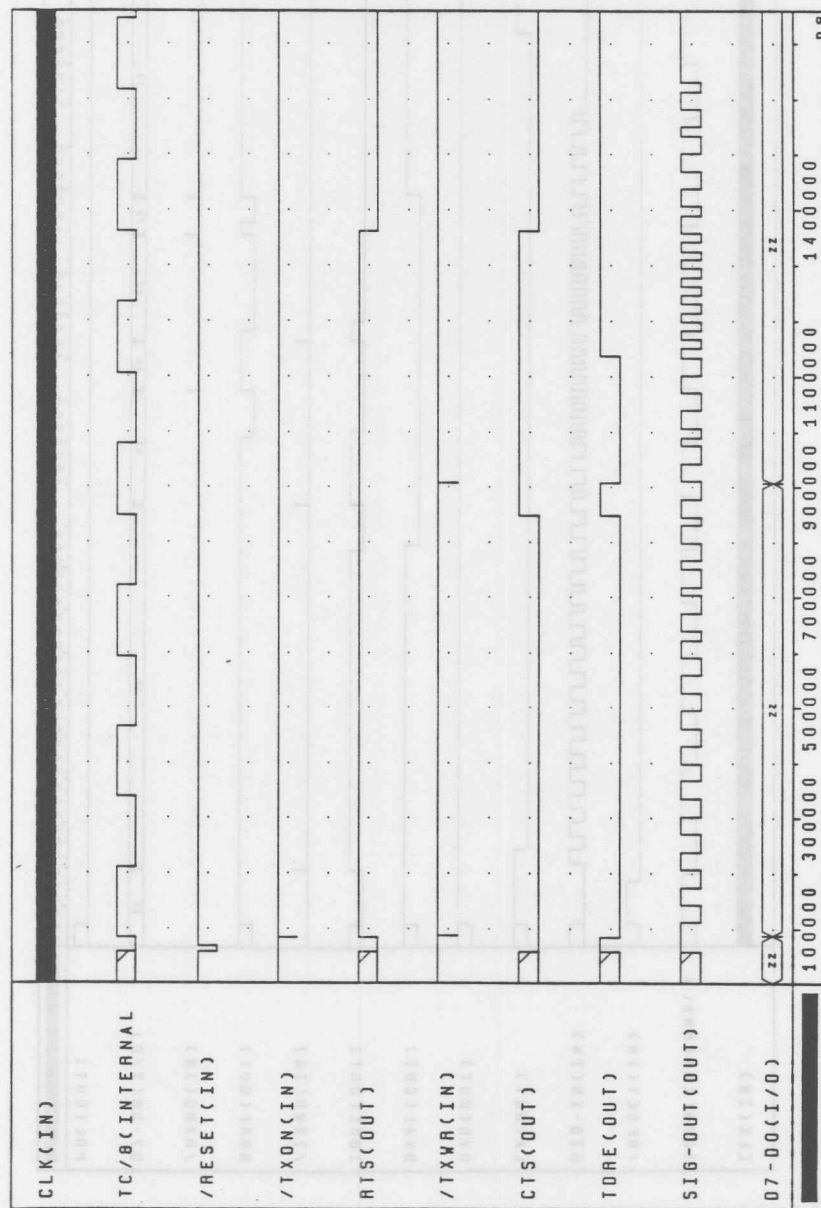


Figure 1 - Transmitter Operation timing diagram

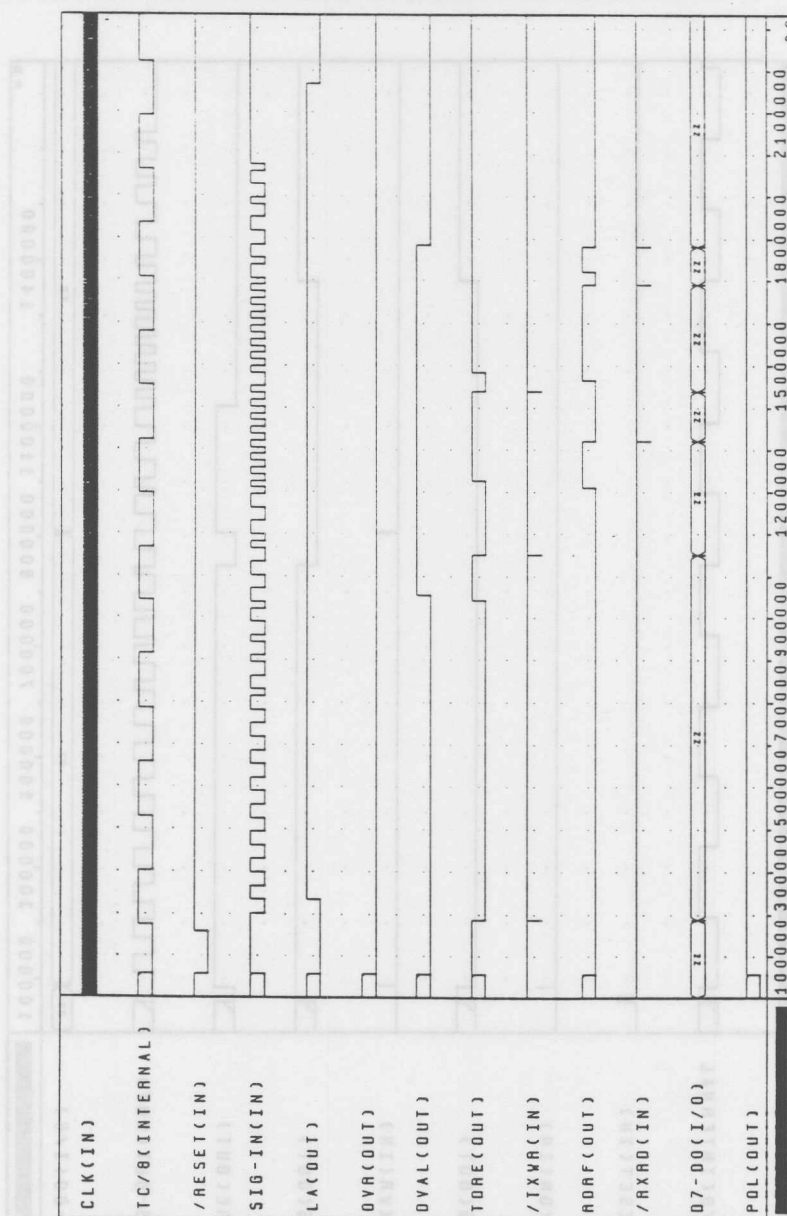


Figure 2 - Transmitter & Receiver timing diagram

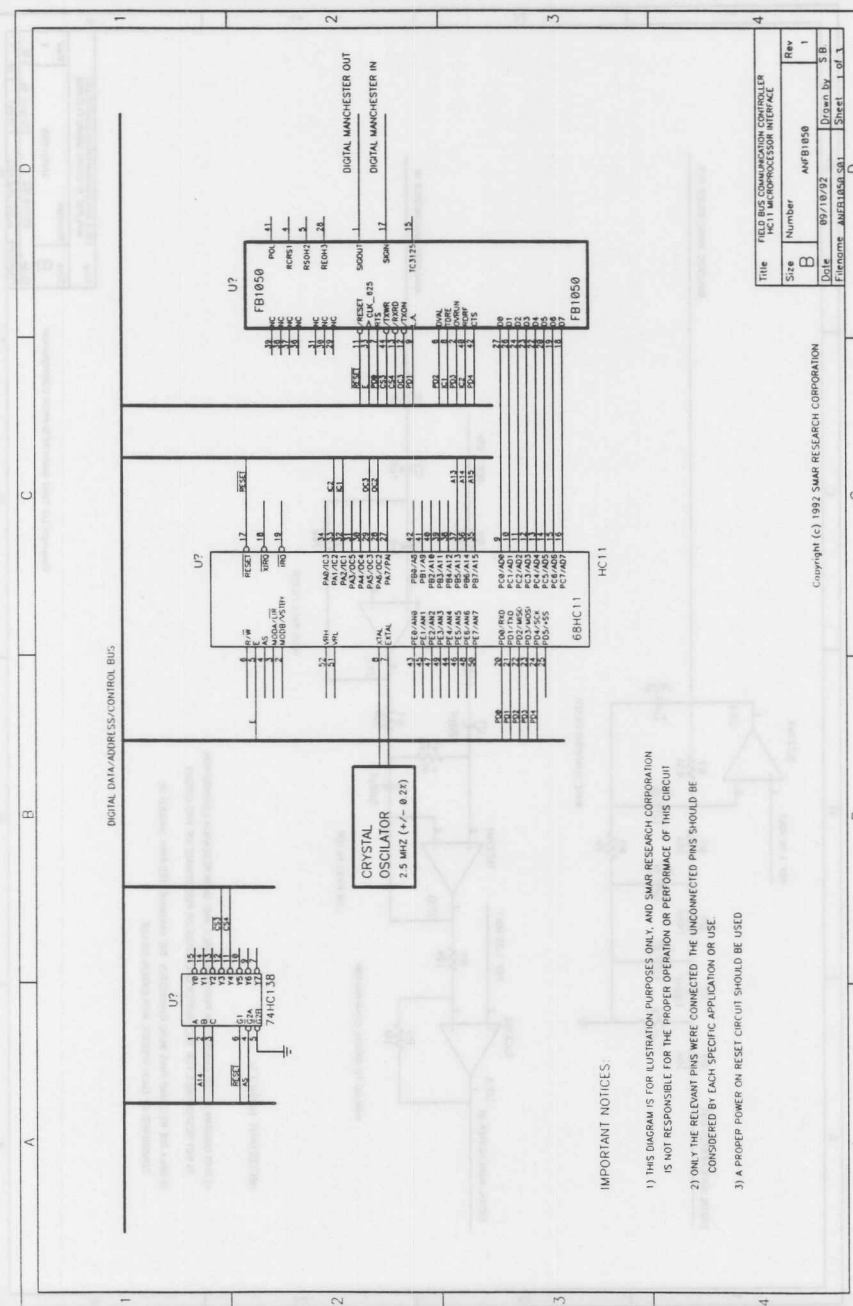
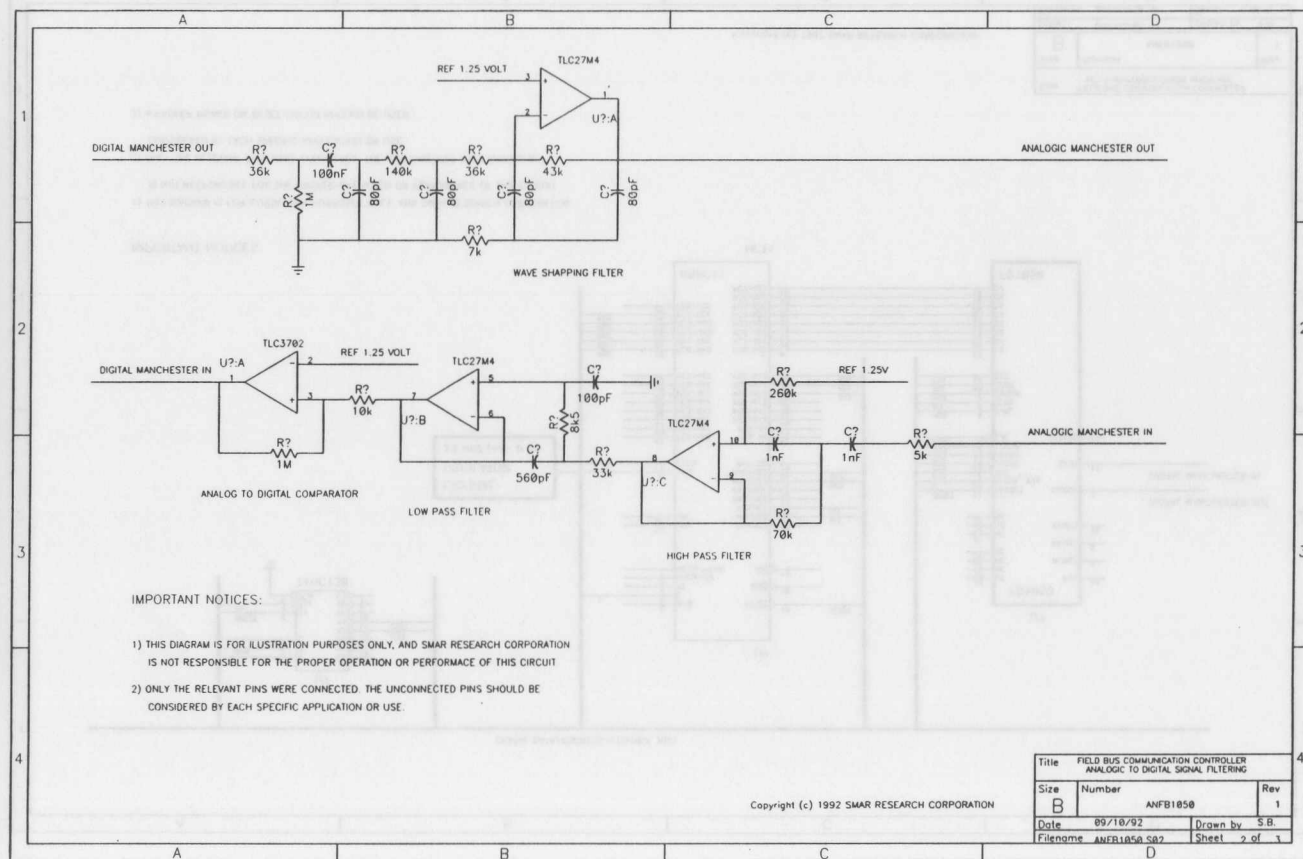


Figure 3 - HC11 to FB1050 Electronic Interface



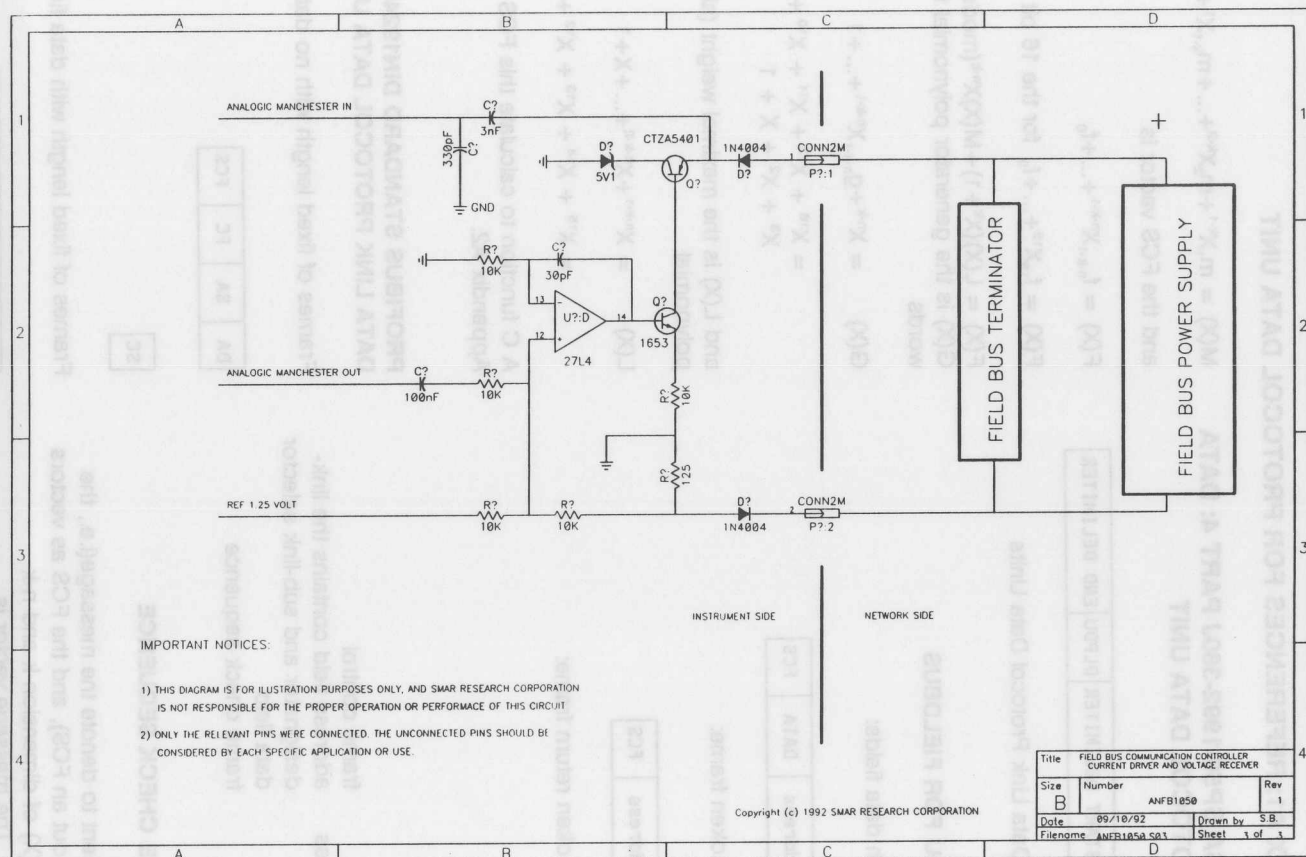


Figure 5 - M.A.U. Current Driver & Voltage Receiver

APPENDIX A1: REFERENCES FOR PROTOCOL DATA UNIT

DRAFT ISA SP50-1992-360J PART 4: DATA LINK PROTOCOL DATA UNIT

PREAMBLE	START DELIMITER	DLPDU	END DELIMITER
----------	-----------------	-------	---------------

DLPDU = Data Link Protocol Data Units

THE DLPDU FOR FIELDBUS

Frames with data fields:

FC	DL_Address	DATA	FCS
----	------------	------	-----

Delegated token frame:

FC	DL_Address	FCS
----	------------	-----

Delegated token return frame:

FC	FCS
----	-----

where:

FC	frame control
DL_Address	address field contains the link-designator and sub-link selector
DATA	data field
FCS	frame check sequence

THE FRAME CHECK SEQUENCE

It is convenient to denote the message(i.e., the DLPDU without an FCS), and the FCS as vectors $M(X)$ and $F(X)$ of dimension k and $n-k$ respectively. The message vector is

$$M(X) = m_1X^{k-1} + m_2X^{k-2} + \dots + m_{k-1}X^1 + m_k$$

and the FCS vector is

$$F(X) = f_{n-k-1}X^{n-k-1} + \dots + f_0$$

$$F(X) = f_{15}X^{15} + \dots + f_0 \text{ for the 16 bit FCS}$$

$F(X) = L(X)(X^k + 1) + M(X)X^{n-k} \pmod{G(X)}$ where $G(X)$ is the generator polynomial for the code words

$$G(X) = X^{n-k} + g_{n-k-1}X^{n-k-1} + \dots + 1$$

$$= X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^6 + X^3 + X^2 + X + 1$$

and $L(X)$ is the maximal weight (all ones) polynomial

$$L(X) = X^{n-k-1} + X^{n-k-2} + \dots + X + 1$$

$$= X^{15} + X^{14} + X^{13} + X^{12} + \dots + X + 1$$

A C function to calculate this FCS is given in Appendix A2.

PROFIBUS STANDARD DIN19245 PART 1: DATA LINK PROTOCOL DATA UNIT

Frames of fixed length with no data field:

DA	SA	FC	FCS
----	----	----	-----

SC

Frames of fixed length with data field:

DA	SA	FC	DATA	FCS
----	----	----	------	-----

Frames with variable data field length:

DA	SA	FC	DATA var_Length	FCS
----	----	----	-----------------	-----

where:

DA Destination Address
 SA Source Address
 SC Single Character, value: E5H
 FC Frame Control
 FCS Frame Check Sequence (FCS is
 calculated from the arithmetic sum of DA,
 SA, and FC.)

DATA Data Field 8 octets
 DATA var_length Data Field variable
 length 246 octets max.

APPENDIX A2: C FUNCTION TO CALCULATE THE FCS (ISA DRAFT)

```
#include <stdio.h>
#define NULL      0
#define BYTE_LENGTH  8
#define HIGH_BYTE(x) ((x & 0xFF00) >> BYTE_LENGTH) /* High order byte */
#define LOW_BYTE(x)  (x & 0x00FF) /* Low order byte */
```

```
/*-----fcs look up table-----*/
```

```
const unsigned int fcs_table[256] =
```

```
{
    0x0000, 0x1DCF, 0x3B9E, 0x2651, 0x773C, 0x6AF3, 0x4CA2, 0x516D,
    0xEE78, 0xF3B7, 0xD5E6, 0xC829, 0x9944, 0x848B, 0xA2DA, 0xBF15,
    0xC13F, 0xDCf0, 0xFAA1, 0xE76E, 0xB603, 0xABCC, 0x8D9D, 0x9052,
    0x2F47, 0x3288, 0x14D9, 0x0916, 0x587B, 0x45B4, 0x63E5, 0x7E2A,

    0x9FB1, 0x827E, 0xA42F, 0xB9E0, 0xE88D, 0xF542, 0xD313, 0xCEDC,
    0x71C9, 0x6C06, 0x4A57, 0x5798, 0x06F5, 0x1B3A, 0x3D68, 0x20A4,
    0x5E8E, 0x4341, 0x6510, 0x78DF, 0x29B2, 0x347D, 0x122C, 0x0FE3,
    0xB0F6, 0xAD39, 0x8B68, 0x96A7, 0xC7CA, 0xDA05, 0xFC54, 0xE198,

    0x22AD, 0x3F62, 0x1933, 0x04FC, 0x5591, 0x485E, 0x6E0F, 0x73C0,
    0xCCD5, 0xD11A, 0xF74B, 0xEA84, 0xBBE9, 0xA626, 0x8077, 0x9DB8,
    0xE392, 0xFE5D, 0xD80C, 0xC5C3, 0x94AE, 0x8961, 0xAF30, 0xB2FF,
    0x0DEA, 0x1025, 0x3674, 0x2BBB, 0x7AD6, 0x6719, 0x4148, 0x5C87,

    0xBD1C, 0xA0D3, 0x8682, 0x9B4D, 0xCA20, 0xD7EF, 0xF1BE, 0xEC71,
    0x5364, 0x4EAB, 0x68FA, 0x7535, 0x2458, 0x3997, 0x1FC6, 0x0209,
    0x7C23, 0x61EC, 0x47BD, 0x5A72, 0x0B1F, 0x16D0, 0x3081, 0x2D4E,
    0x925B, 0x8F94, 0xA9C5, 0xB40A, 0xE567, 0xF8A8, 0xDEF9, 0xC336,

    0x455A, 0x5895, 0x7EC4, 0x630B, 0x3266, 0x2FA9, 0x09F8, 0x1437,
    0xAB22, 0xB6ED, 0x90BC, 0x8D73, 0xDC1E, 0xC1D1, 0xE780, 0xFA4F,
    0x8465, 0x99AA, 0xBFFB, 0xA234, 0xF359, 0xEE96, 0xC8C7, 0xD508,
    0x6A1D, 0x77D2, 0x5183, 0x4C4C, 0x1D21, 0x00EE, 0x26BF, 0x3B70,

    0xDAEB, 0xC724, 0xE175, 0xFCBA, 0xADD7, 0xB018, 0x9649, 0x8B86,
    0x3493, 0x295C, 0x0F0D, 0x12C2, 0x43AF, 0x5E60, 0x7831, 0x65FE,
    0x1BD4, 0x061B, 0x204A, 0x3D85, 0x6CE8, 0x7127, 0x5776, 0x4AB9,
    0xF5AC, 0xE863, 0xCE32, 0xD3FD, 0x8290, 0x9F5F, 0xB90E, 0xA4C1,
```

0x67F7, 0x7A38, 0x5C69, 0x41A6, 0x10CB, 0x0D04, 0x2B55, 0x369A,
 0x898F, 0x9440, 0xB211, 0xAFDE, 0xFEB3, 0xE37C, 0xC52D, 0xD8E2,
 0xA6C8, 0xBB07, 0x9D56, 0x8099, 0xD1F4, 0xCC3B, 0xEA6A, 0xF7A5,
 0x48B0, 0x557F, 0x732E, 0x6EE1, 0x3F8C, 0x2243, 0x0412, 0x19DD,

0xF846, 0xE589, 0xC3D8, 0xDE17, 0x8F7A, 0x92B5, 0xB4E4, 0xA92B,
 0x163E, 0x0BF1, 0x2DA0, 0x306F, 0x6102, 0x7CCD, 0x5A9C, 0x4753,
 0x3979, 0x24B6, 0x02E7, 0x1F28, 0x4E45, 0x538A, 0x75DB, 0x6814,
 0xD701, 0xCACE, 0xEC9F, 0xF150, 0xA03D, 0xBDF2, 0x9BA3, 0x866C

```
};
```

```
/*-----*/
/*
/* PURPOSE: This function computes the FCS for a given string. */
/*
/* INPUTS: A pointer to the string, and string length. */
/*
/* RETURNS: A pointer to the computed FCS. */
/*-----*/
```

```
unsigned char *compute_fcs(unsigned char *pdu_ptr, unsigned char pdu_length)
```

```
{
  unsigned short int fcs;
  unsigned short int temp_fcs;
  unsigned char *byte_ptr;
  unsigned char *fcs_ptr;
  unsigned int i;
```

```
/*----- calculate FCS -----*/
```

```
fcs = NULL;
byte_ptr = (unsigned char *)pdu_ptr;
for (i=0; i<pdu_length; i++){
```

```
  temp_fcs = fcs_table[( *byte_ptr++ ) ^ HIGH_BYTE(fcs)];
  fcs = ((HIGH_BYTE(temp_fcs) ^ LOW_BYTE(fcs)) <<
  BYTE_LENGTH) | LOW_BYTE(temp_fcs);
```

```
}
fcs_ptr[0] = HIGH_BYTE(fcs);
fcs_ptr[1] = LOW_BYTE(fcs);
return(fcs_ptr);
}
```

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